UNIVERSIDADE FEDERAL DO RIO DE JANEIRO

CONCURSO PÚBLICO

ENGENHEIRO ELETRÔNICO

INSTRUÇÕES GERAIS

- ♦ Você recebeu do fiscal:
  - ♦ Um caderno de questões contendo 65 (sessenta e cinco) questões de múltipla escolha da Prova Objetiva;
  - ♦ Um cartão de respostas personalizado para a Prova Objetiva.
- ♦ É responsabilidade do candidato certificar-se de que o nome do cargo informado nesta capa de prova corresponde ao nome do cargo informado em seu cartão de respostas.
- ♦ Ao ser autorizado o início da prova, verifique, no caderno de questões, se a numeração das questões e a paginação estão corretas.
- ♦ Você dispõe de 4 (quatro) horas para fazer esta Prova. Faça-a com tranquilidade, mas controle o seu tempo. Esse tempo inclui a marcação do cartão de respostas.
- ♦ Após o início da prova, será efetuada a coleta da impressão digital de cada candidato (Edital 90/2010 – subitem 9.9).
- ♦ Somente após decorrida uma hora do início da prova, o candidato poderá entregar o seu caderno de questões, o seu cartão de respostas, e retirar-se da sala de prova (Edital 90/2010 – subitem 9.11.7, alínea “a”).
- ♦ Após o término de sua prova, entregue obrigatoriamente ao fiscal o cartão de respostas devidamente assinado e o caderno de respostas (Edital 90/2010 – subitem 9.11.7, alínea “d”).
- ♦ Somente será permitido levar seu caderno de questões faltando uma hora para o término estabelecido para o fim da prova (Edital 90/2010 – subitem 9.11.7, alínea “b”).
- ♦ É terminantemente vedado copiar seus assinalamentos feitos no cartão de respostas (Edital 90/2010 – subitem 9.11.7, alínea “c”).
- ♦ Os 3 (três) últimos candidatos de cada sala só poderão ser liberados juntos (Edital 90/2010 – subitem 9.11.7, alínea “e”).
- ♦ Se você precisar de algum esclarecimento, solicite a presença do responsável pelo local.
- ♦ Transcreva a frase abaixo, utilizando letra cursiva, no espaço reservado no canto superior direito do seu cartão de respostas.

> *“O descontentamento é o primeiro passo na evolução de um homem ou de uma nação.”*
>
> Oscar Wilde

INSTRUÇÕES ESPECÍFICAS

- ♦ Verifique se os seus dados estão corretos no cartão de respostas. Se necessário, solicite ao fiscal a correção na Ata de Aplicação de Prova.
- ♦ Leia atentamente cada questão e assinale no cartão de respostas a alternativa que mais adequadamente a responde.
- ♦ O cartão de respostas NÃO pode ser dobrado, amassado, rasurado, manchado ou conter qualquer registro fora dos locais destinados às respostas.
- ♦ A maneira correta de assinalar a alternativa no cartão de respostas é cobrindo, fortemente, com caneta esferográfica de tinta indelével azul ou preta (Edital 90/2010 – subitem 9.11.4), o espaço a ela correspondente, conforme o exemplo a seguir:

Ⓐ ● Ⓒ Ⓓ Ⓔ

Cronograma Previsto (Cronograma completo no endereço www.nce.ufrj.br/concuros)

Atividade	Data	Local
Divulgação do gabarito preliminar	14/02/11	www.nce.ufrj.br/concursos
Interposição de recursos contra o gabarito preliminar	15 e 16/02/11	www.nce.ufrj.br/concursos
Divulgação do resultado do julgamento dos recursos contra o gabarito preliminar	22/02/11	www.nce.ufrj.br/concursos
Divulgação do resultado preliminar da Prova	22/02/11	www.nce.ufrj.br/concursos

LÍNGUA PORTUGUESA

TEXTO

DEIXEM OS CÉREBROS SAIR

Michael Clemens

- A emigração de profissionais qualificados não é perda, mas estímulo à educação e à economia -

“Fuga de cérebros” é uma expressão comum para descrever nas nações em desenvolvimento a saída de profissionais qualificados, como médicos e engenheiros, em busca de dinheiro ou melhores oportunidades em outros países. Muitos especialistas dizem que esse processo suga os maiores talentos de um país. No entanto, hoje um grande volume de pesquisas mostra que o fluxo de profissionais para o exterior pode na verdade beneficiar as duas partes. A ideia de que esse tipo de emigração corresponde necessariamente a uma perda de cérebros é simplesmente um mito.

Pegue o caso das Filipinas. O país envia mais enfermeiras para o exterior que qualquer outro em desenvolvimento, ainda assim, tem mais enfermeiras per capita em casa do que países bem mais ricos, como o Reino Unido. O que ocorre é que a perspectiva de ganhar muito mais no exterior leva mais filipinos a estudar para conseguir um diploma de enfermagem. Consequentemente, há um aumento líquido no número total de enfermeiras nas Filipinas, mesmo se você levar em conta aquelas que saíram do país. E fenômenos semelhantes acontecem em outros países onde há um grande aumento na emigração de mão de obra qualificada.

1 - O título do texto:

(A) contraria o lugar-comum de que é prejuízo para um país a “fuga de cérebros”;
(B) funciona como uma expressão absurda que atrai a atenção dos leitores;
(C) apóia a política de emigração adotada por países em desenvolvimento;
(D) atua como incentivo à procura de melhores salários no exterior;
(E) serve de pedido de atenção para uma política equivocada em países pobres.

2 - De forma metonímica, o vocabulário “cérebros” significa no texto acima:

(A) pessoas superdotadas;
(B) profissionais qualificados;
(C) técnicos de nível médio;
(D) empregados de empresas estatais;
(E) indivíduos mal renumerados.

3 - No título do texto há um exemplo de emprego correto do verbo *deixar*. A frase a seguir que apresenta erro no emprego desse mesmo verbo é:

(A) o país os deixava entrar;
(B) a lei deixava-o viajar sozinho;
(C) os pais deixaram-lhe uma herança;
(D) os filipinos deixaram-lhe emigrar;
(E) o diploma não a deixava exercer a profissão.

4 - O vocábulo *emigração* tem como parônimo *imigração*, de valor semântico oposto. A frase abaixo que deve ser preenchida com a primeira das formas entre parênteses é:

1. o furto de pequenos objetos no colégio sempre passou __________. (desapercebido - despercebido);
2. sua __________, o cardeal, rezou a missa da formatura dos alunos. (Iminência – Eminência);
3. a polícia invadiu a casa, mas não possuía um __________ de busca. (mandato – mandado);
4. pretendia __________ o submarino logo que deixasse o porto. (emergir – imergir);
5. aconteceu um __________ grave na Rio-São Paulo. (acidente – incidente).

5 - *"Fuga de cérebros" é uma expressão comum para descrever nas nações em desenvolvimento a saída de profissionais qualificados, como médicos e engenheiros, em busca de dinheiro ou melhores oportunidades em outros países.* Infere-se desse segmento do texto que:

(A) a expressão "fuga de cérebros" só é conhecida nos países em desenvolvimento;
(B) médicos e engenheiros são os profissionais que mais emigram para outros países;
(C) um dos motivos da saída de cérebros é a procura de melhor nível de vida;
(D) a saída de cérebros é uma atividade ilegal;
(E) muitos profissionais não qualificados também imigram para países em desenvolvimento.

6 - *"Fuga de cérebros" é uma expressão comum para descrever nas nações em desenvolvimento a saída de profissionais qualificados, como médicos e engenheiros, em busca de dinheiro ou melhores oportunidades em outros países.* Nesse segmento inicial do texto, o trecho de "é uma expressão" até "profissionais qualificados", em relação ao termo anterior, funciona como:

(A) exemplificação;
(B) enumeração;
(C) tradução;
(D) explicação;
(E) retificação.

7 - A opinião dada pelos "especialistas", no segundo período do texto:

(A) apóia argumentativamente a tese do autor do texto;
(B) exemplifica um tipo de "fuga de cérebros";
(C) contraria o pensamento exposto no texto;
(D) serve de testemunho de autoridade para o enunciador do texto;
(E) apresenta uma ironia sobre uma opinião falsa.

8 - *Muitos especialistas dizem que esse processo suga os maiores talentos de um país.* A afirmativa INADEQUADA sobre os componentes desse segmento do texto é:

(A) o pronome indefinido *muitos* indica uma grande quantidade não determinada;
(B) o vocábulo *especialistas* se refere a pessoas de grande saber em um terreno específico;
(C) o pronome demonstrativo *esse* é empregado em referência a algo anteriormente expresso;
(D) o vocábulo *processo* se refere à busca de dinheiro e melhores oportunidades em outro país;
(E) o vocábulo *talentos* se relaciona a cérebros.

9 - "No entanto, hoje um grande volume de pesquisas mostra..."; o conectivo a seguir que pode substituir adequadamente o que está sublinhado nesse segmento do texto é:

(A) no entretanto;
(B) apesar disso;
(C) desse modo;
(D) logo;
(E) contudo.

10 - *"...um grande volume de pesquisas mostra que o fluxo de profissionais para o exterior pode na verdade beneficiar as duas partes".* As "duas partes" referidas nessa frase do texto se referem a:

(A) busca de dinheiro e de melhores oportunidades;
(B) emigrantes e os imigrantes;
(C) países em desenvolvimento e os cérebros;
(D) países desenvolvidos e os países em desenvolvimento;
(E) cérebros e os países desenvolvidos.

11 - *"...um grande volume de pesquisas mostra que o fluxo de profissionais para o exterior pode na verdade beneficiar as duas partes".* Nesse segmento do texto, a expressão "na verdade" só NÃO pode ser adequadamente substituída por:

(A) de fato;
(B) certamente;
(C) seguramente;
(D) na realidade;
(E) possivelmente.

12 - Assinale a alternativa em que a correspondência entre os verbos do texto e seus adjetivos cognatos está EQUIVOCADA:

(A) beneficiar – beneficiente;
(B) descrever – descritivo;
(C) estudar – estudioso;
(D) sugar – sugador;
(E) corresponder – correspondente.

13 - No trecho *"A ideia de que esse tipo de emigração corresponde necessariamente a uma perda de cérebros é simplesmente um mito"*, o vocábulo simplesmente é um modalizador, ou seja, um vocábulo por meio do qual o enunciador manifesta determinada atitude em relação ao conteúdo do seu próprio enunciado.

A frase a seguir em que o vocábulo sublinhado pode ser classificado como modalizador é:

(A) infelizmente muitos países perdem cérebros importantes;
(B) pegue o caso recente do Haiti;
(C) desconsidere o caso de países pobres;
(D) cremos que nunca mais o veremos;
(E) agiu covardemente naquela situação difícil.

14 - *O país envia mais enfermeiras para o exterior que qualquer outro em desenvolvimento, ainda assim, tem mais enfermeiras per capita em casa do que países bem mais ricos*. No caso dos termos sublinhados, podemos dizer que:

(A) todos possuem o mesmo valor semântico;
(B) só os dois primeiros têm o mesmo valor semântico;
(C) só o primeiro e o terceiro têm o mesmo valor semântico;
(D) o primeiro apresenta valor semântico diferente dos outros dois;
(E) os três apresentam valor semântico distinto.

15 - *"...tem mais enfermeiras per capita em casa..."*; a expressão latina destacada significa:

(A) nas cidades principais;
(B) com emprego fixo;
(C) por cada indivíduo;
(D) já formadas;
(E) de formação especializada.

16 - Segundo o texto, o fato que leva a haver bastantes enfermeiras nas Filipinas é:

(A) a atração pelo trabalho no Reino Unido;
(B) os melhores salários dessa profissão;
(C) a grande necessidade dessas profissionais nas Filipinas;
(D) a perspectiva de ir para o exterior e progredir;
(E) a imensa quantidade de enfermos nos países subdesenvolvidos.

17 - O exemplo das Filipinas serve textualmente para:

(A) enumerar vários casos de “fuga de cérebros”;
(B) comparar as Filipinas ao Reino Unido;
(C) denunciar uma injusta “fuga de cérebros”;
(D) chamar atenção sobre uma injustiça social;
(E) apoiar uma tese anteriormente expressa.

18 - “...acontecem em outros países onde há um grande aumento na emigração...”; o pensamento abaixo em que houve troca INDEVIDA entre *onde* e *aonde* é:

(A) “Não importa aonde você vá, você estará lá.” (Saul Gorn);
(B) “O mistério não é um muro aonde a inteligência esbarra, mas um oceano onde ela mergulha.” (Gustave Thibon);
(C) “O bom não é bom onde o ótimo é esperado.” (Thomas Fuller);
(D) “Não olhe onde você caiu, mas onde você escorregou.” (Provérbio liberiano);
(E) “Só Deus sabe aonde se dirige sua vida.” (Nouailles).

19 - “Deixem os cérebros sair”; a frase a seguir que apresenta um sentido diferente dessa frase do texto é:

(A) pemitam a saída dos cérebros;
(B) deixem que os cérebros saiam;
(C) dêem permissão para a saída dos cérebros;
(D) a saída deve ser deixada pelos cérebros;
(E) permita-se aos cérebros a saída.

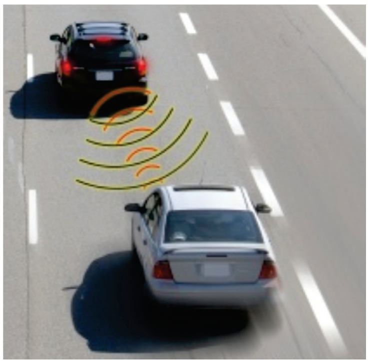
20 - O texto lido localiza-se numa seção da revista Superinteressante, denominada “Polêmica”. Com esse título já se pode antever que os textos aí colocados devem ser do tipo:

(A) descritivo;
(B) informativo;
(C) publicitário;
(D) argumentativo;
(E) narrativo.

LÍNGUA INGLESA

READ TEXT I AND ANSWER QUESTIONS 21 TO 25:

Automotive radar coming to cheaper cars



Automotive radar systems using chips from Analog Devices and others use both front- and rear-facing units for collision avoidance and blind-spot detection, respectively.

Radar Technology has registered on automakers' own radar for more than a decade, though the car manufacturers have proceeded with their typical caution in adopting what has been a costly technology with safety implications. But as silicon sensor costs come down and as the technology gains traction in luxury models, radar systems will begin to trickle down over the next few years to midpriced autos. Lower silicon and system prices will also encourage more governments to mandate automotive radar.

Going into 2011, automotive radar already offers collision avoidance and mitigation in the forward-facing direction, as well as blind-spot monitoring and parking support via rear-facing radar. Beyond 2011, the technology will eventually enable driverless freeway motoring, with smart algorithms using forward- and rear-facing radar, as well as lane detection systems, to control drive-by-wire steering, acceleration and braking systems.

(http://www.eetimes.com/electronics-news/4211508/10-technologies-to-watch-in-2011?pageNumber=4)

21 - The text is about:

(A) the costs and the advantages of using radars in cars;
(B) technology which will be exclusive to expensive cars;
(C) different types of radars available for sale ten years ago;
(D) lack of governmental support for radar manufacturing;
(E) the dangers of using radars in all kinds of cars.

22 - The opening sentence "Radar Technology has registered on automakers' own radar for more than a decade" implies that car manufacturers have:

(A) refused to use radar technology in cheaper cars;
(B) always been uninformed about radar technology;
(C) been responsible for reducing accidents on roads;
(D) long been aware of automotive radar technology;
(E) warned about the risks of automakers` radars.

23 - According to the text, "blind-spot monitoring" (l. 9):

(A) helps lower the price of costly modern cars;
(B) optimizes automotive acceleration system;
(C) aids the performance of automotive traction;
(D) keeps in check areas invisible to the driver;
(E) traces the complete route for the driver.

24 - The underlined expression in "But as silicon sensor costs <u>come down</u>" can be replaced by:

(A) increase;
(B) lower;
(C) stop;
(D) rise;
(E) disappear.

25 - The sentence "Beyond 2011, the technology will eventually enable driverless freeway motoring" (l. 10/11) offers a(n):

(A) instruction;
(B) complaint;
(C) advice;
(D) guarantee;
(E) prediction.

READ TEXT II AND ANSWER QUESTIONS 26 TO 30:

TEXT II

A new field is emerging in electronics that will be a giant leap in computer and electronics science. It is the field of quantum computing and quantum technology. Quantum computing is area of scientific knowledge aimed at developing computer technology based on the principles of quantum theory. In quantum computing the "qbit" instead of the traditional bit of information is used. Traditionally, a bit can assume two values: 1 and 0. All the computers up-to-date are based on the "bit" principle. However, the new "qbit" is able to process anything between 0 and 1. This implies that new types of calculations and high processing speeds can be achieved.

Quantum computers have been more of a research area until now. But recently, the first quantum computer has been built in the United States, according to a recent paper published on the prestigious scientific journal Nature Physics. This new computer is said to achieve unseen processing speeds to the tune of a billion times per second, making this the fastest chip on earth.

We are bound to see many nanotechnological applications within the electronic industry in the near future. These will undoubtedly increase the quality of life of our society.

(from http://www.brighthub.com/engineering/electrical/articles/7761.aspx#ixzz18leJwisW)

26 - According to the text, the use of quantum theory in computer science may lead to the:

(A) increase of speed in data processing;
(B) decrease of computer manufacturing;
(C) return to earlier forms of calculation;
(D) neglect of advances in nanotechnology;
(E) worsening of environmental conditions.

27 - In the text, the expression "a giant leap" (l. 1) refers to:

(A) electronics science;
(B) computer science;
(C) quantum theory;
(D) computer technology;
(E) quantum computing.

28 - Instead of in "instead of the traditional bit of information" (l. 4) signals a(n):

(A) concession;
(B) completion;
(C) substitution;
(D) illustration;
(E) addition.

29 - The underlined word in "<u>unseen</u> processing speeds" (l. 9) can be replaced by:

(A) unbearable;
(B) unprecedented;
(C) uneven;
(D) unexciting;
(E) unexplained .

30 - In "These will undoubtedly increase" (l. 12) the author expresses:

(A) distrust;
(B) anger;
(C) fear;
(D) sorrow;
(E) certainty.

REGIME JURÍDICO ÚNICO

31 - Em relação aos requisitos básicos para investidura em cargo público dos servidores regidos pela Lei 8112/90, as universidades federais poderão, prover em sua totalidade, cargos com:

(A) médicos, técnicos e cientistas brasileiros;
(B) cientistas brasileiros, cientistas estrangeiros e procuradores;
(C) estagiários, médicos e cientistas;
(D) residentes, estagiários e procuradores;
(E) residentes, técnicos e cientistas estrangeiros.

32 - Manoel é servidor público federal lotado na UFBA, regido pelo regime jurídico único dos servidores da União. Em 15 de maio de 2010 foi cedido para exercer suas atribuições na UFRJ. Compulsando os limites estabelecidos para o retorno do seu exercício funcional, após a publicação do ato, o servidor terá:

(A) no mínimo quinze e no máximo trinta dias de prazo para a retomada do efetivo desempenho das atribuições do cargo;
(B) no mínimo quinze e no máximo quarenta e cinco dias de prazo para a retomada do efetivo desempenho das atribuições do cargo;
(C) no mínimo dez e no máximo trinta dias de prazo para a retomada do efetivo desempenho das atribuições do cargo;
(D) no mínimo trinat e no máximo sessenta e cinco dias de prazo para a retomada do efetivo desempenho das atribuições do cargo;
(E) no mínimo dez e no máximo vinte e cinco dias de prazo para a retomada do efetivo desempenho das atribuições do cargo.

33 - Com base na lei estatutária do servidor público federal, o servidor em estágio probatório poderá obter licenças e afastamentos. Em relação aos tipos de licenças, é legitima sua concessão para:

(A) capacitação;
(B) tratar de interesses particulares;
(C) desempenho de mandato classista;
(D) o serviço militar;
(E) mandato eletivo.

34 - O RJU-Lei 8112/90 assegura ao servidor o direito de petição, em requerer aos Poderes Públicos, créditos resultantes das relações de trabalho, sempre em defesa de direito ou interesse legítimo. Na hipótese de indeferimento em seu requerimento, caberá na forma da lei:

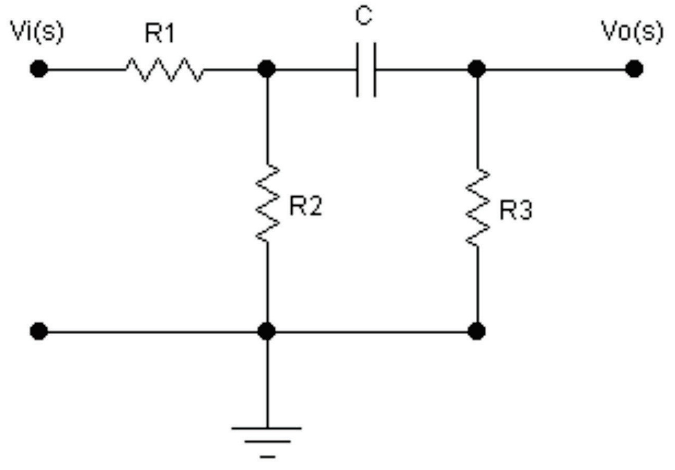
(A) recurso à autoridade que expediu o ato ou proferiu a primeira decisão;
(B) recurso à autoridade imediatamente superior a quem expediu o ato ou proferiu a primeira decisão;
(C) recurso à autoridade superior a quem expediu o ato ou proferiu a primeira decisão;
(D) pedido de reconsideração à autoridade imediatamente superior a que expediu o ato ou proferiu a primeira decisão;
(E) pedido de reconsideração à autoridade que expediu o ato ou proferiu a primeira decisão.

35 - No trâmite do processo administrativo disciplinar do serviço público federal, aos servidores regidos pela lei estatutária, considerar-se-á revel o indiciado que, regularmente citado, não apresentar defesa no prazo legal. Assim, a revelia será declarada, por termo, nos autos do processo e devolverá o prazo para a defesa. Para defender o indiciado revel, a autoridade instauradora do processo designará um:

(A) Defensor Dativo, ocupante de cargo público efetivo;
(B) Defensor Público, encaminhado pelo MPF;
(C) Defensor Bacharel em Direito, encaminhado pela OAB;
(D) Procurador Federal;
(E) Advogado da União.

CONHECIMENTOS ESPECÍFICOS

36 - No circuito abaixo, usado como atenuador, R1=R2= 10,0 kΩ, R3= 5,0 kΩ e o capacitor C = 10,0 nF (nano Farad).



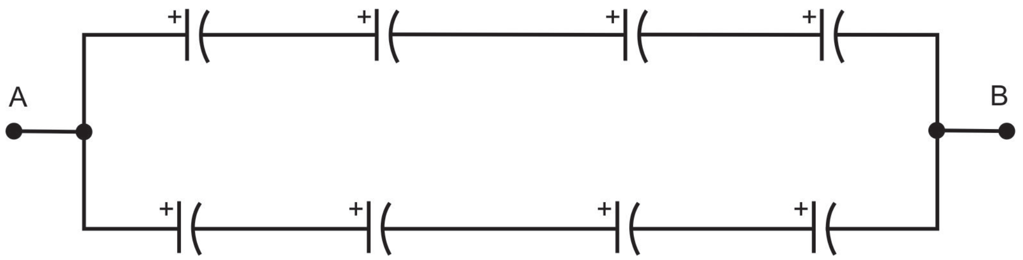
Sendo Vi(s) uma tensão senoidal de amplitude constante e frequência variável, a função de transferência Vo(s)/Vi(s), o caracteriza como um filtro, com freqüência de corte inferior igual a:

(A) 500 rad/s;
(B) 1000 rad/s;
(C) 2000 rad/s;
(D) 5000 rad/s;
(E) 10.000 rad/s.

37 - Na amostragem de um sinal de tensão analógico, com freqüência variável de 100 Hz a 10.000 Hz, é usada uma chave eletrônica comandada por um relógio (clock). Dentre os valores das frequências dadas a seguir, para que se consiga recuperar o sinal analógico amostrado, a mínima freqüência do relógio deverá ser de:

(A) 5000 Hz;
(B) 10.000 Hz;
(C) 15.000 Hz;
(D) 25.000 Hz ;
(E) 40.000Hz.

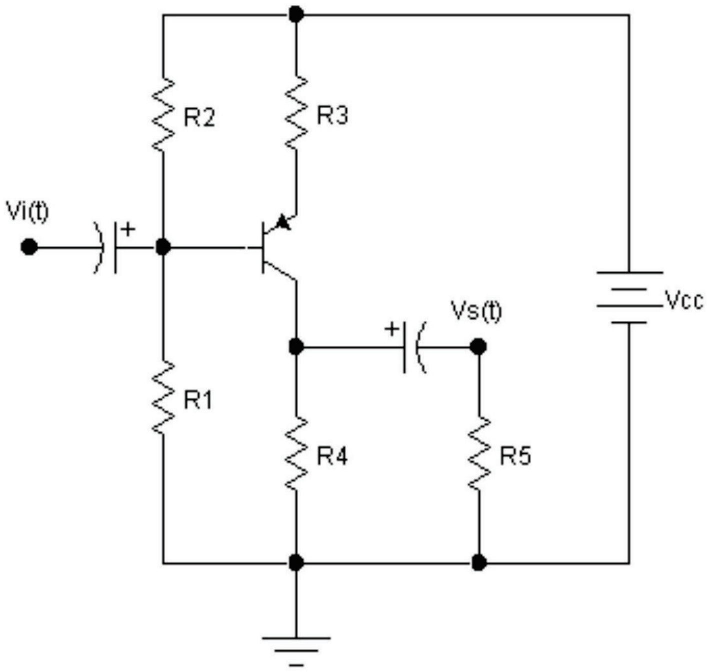
38 - No circuito deste item os capacitores são todos iguais a 10,0 µF (micro Farad) X 100 Volts de isolamento, e a mesma corrente de fuga.



A associação de todos os capacitores entre o ponto "A" e o ponto "B", equivale a um capacitor de:

(A) 5,0 µF x 100 Volts;
(B) 5,0 µF x 400 Volts;
(C) 10,0 µF x 100 V0lts;
(D) 20,0 µF x 200 Volts;
(E) 40,0 µF x 400 V0lts.

39 - No circuito abaixo Vcc = 12 Volts, R1 = 39,0 kΩ, R2 = 4, 7 kΩ, R3 = 1,0 kΩ e R4 = R5 = 5,6 kΩ. O sinal Vi(t) é senoidal com uma frequência em que os capacitores têm reatâncias desprezíveis e o transistor apresenta os parâmetros hie = 1,0 kΩ, hre = 0,0, hoe = 0,0 S e hfe= 300.



O valor mais próximo para o módulo do ganho [Vs(t)/Vi(t)] é:

(A) 2,8;
(B) 5,6;
(C) 60,2;
(D) 150,0;
(E) 298,1.

40 - Ao medir a impedância de uma solução aquosa não saturada de um sal, um químico encontrou o valor: Zs(w) = (30,0 + 20,0 j), usando na medição um gerador senoidal. Querendo aquecer a mesma solução, com o mesmo gerador senoidal calibrado na mesma frequência, a máxima transferência de potência entre o gerador e a solução ocorrerá quando a impedância do gerador for:

(A) Zg(w) = 22,3 Ω;
(B) Zg(w) = 30,0 Ω;
(C) Zg(w) = 36,0 Ω;
(D) Zg(w) = (30,0 + 20,0 j) Ω;
(E) Zg(w) = (30,0 – 20,0 j) Ω.

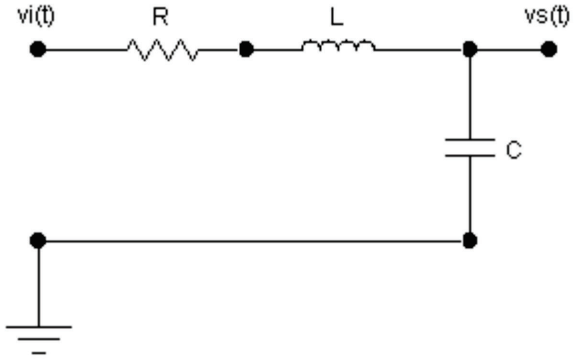
41 - É comum em álgebra Booleana representamos uma função lógica pelos seus mintermos. **X, Y e Z** são variáveis lógicas e **X´, Y´e Z´** os seus complementos. A função a seguir, representada pelos seus mintermos,

F(X,Y,Z) = ∑mi (1, 2, 3, 4, 5, 6, 7) =
= X´. Y´. Z + X´. Y . Z´ + X´. Y. Z + X .Y´. Z´ +
+ X . Y´. Z + X. Y. Z´ + X. Y. Z,

poderá ser simplificada para:

(A) F = X + Y + Z;
(B) F = X´. Y´. Z´;
(C) F = X´+ Y´+ Z´;
(D) F = X. Y´+ X´. Y;
(E) F = X. Y´+ X´. Z.

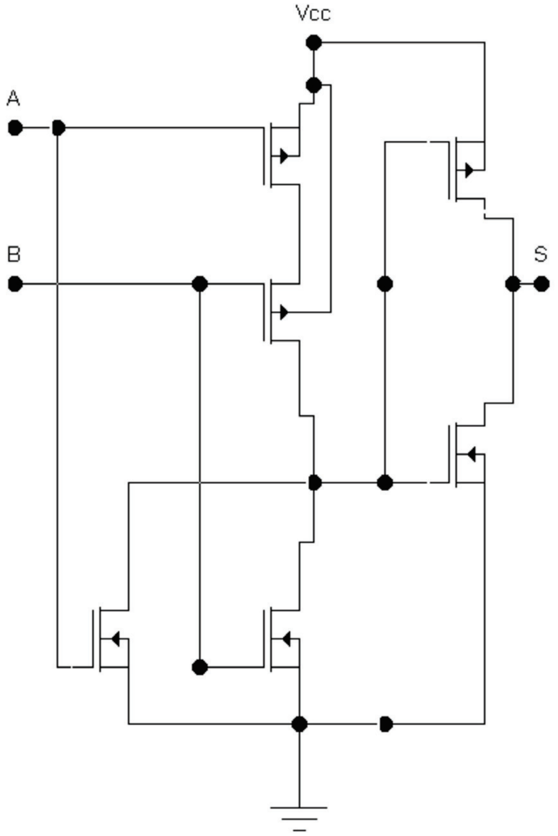
42 - No circuito a seguir o resistor R = 1,0 Ω é a resistência efetiva intrínseca do indutor de indutância L = 10,0 μH (micro Henry). O capacitor C é ideal e tem uma capacitância C = 1,0 nF (nano Farad).



Se a entrada vi(t) = 2. sen 10^7 t (Volts), a tensão máxima (de pico) de vs(t) será igual a:

(A) 2000,0 Volt;
(B) 200,0 Volts;
(C) 100,0 Volts;
(D) 2,0 Volts;
(E) 1,0 Volts.

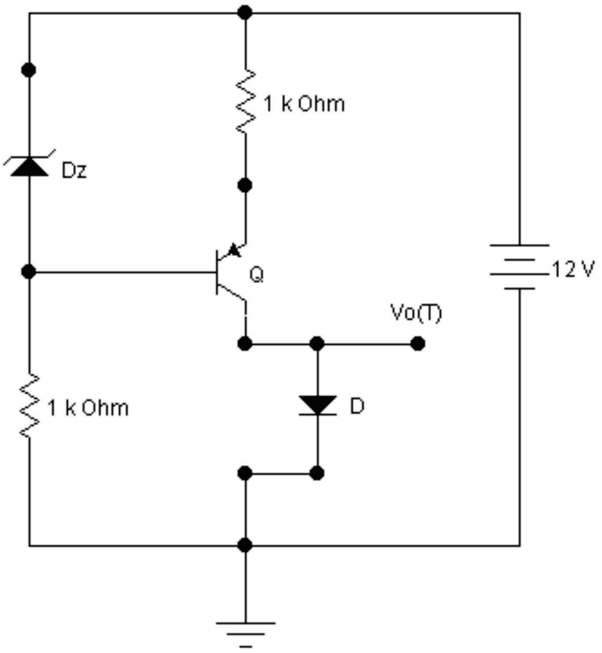
43 - A porta lógica a seguir foi realizada com CMOS (*Complementary-Metal-Oxide-Semiconductor*). As entradas digitais “A” e “B” têm níveis (1) lógicos iguais a +Vcc e níveis (0) lógicos iguais ao potencial da terra.



Nestes termos, podemos afirmar, que, sendo a saída o ponto S, o circuito funciona como uma porta:

(A) Ou-exclusivo;
(B) E;
(C) Não-Ou;
(D) Ou;
(E) Não-E.

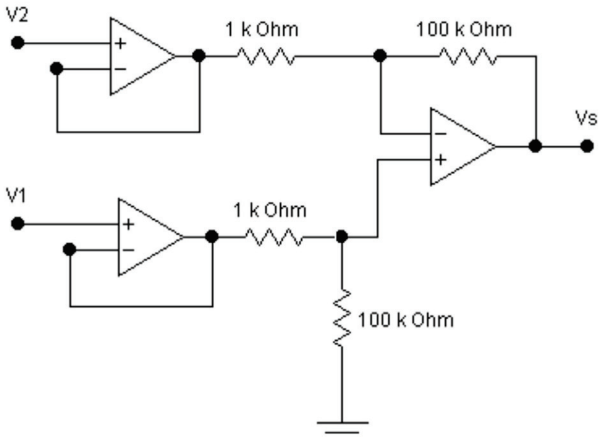
44 - No circuito deste item o diodo D é usado como sonda para medida da temperatura absoluta T, através da medida da tensão Vo(T) referida ao ponto de aterramento, isto é, Vo(T) é uma função da temperatura no diodo. O transistor Q é de silício, o diodo D é de germânio, e Dz é um diodo Zener, de tensão Zener Vz = 4,7 Volts. A corrente de saturação inversa do diodo é constante. Excetuando-se o diodo D, todos os outros componentes do circuito estão a uma temperatura constante.



Podemos afirmar que, sendo “C” uma constante, a tensão Vo(T) é uma função que mais se aproxima da forma:

(A) Vo(T) = C. e $^{40.T}$;
(B) Vo(T) = C.T ;
(C) Vo(T) = C.T$^{1/2}$;
(D) Vo(T) = C.T^{2} ;
(E) Vo(T) = C.T^{3}.

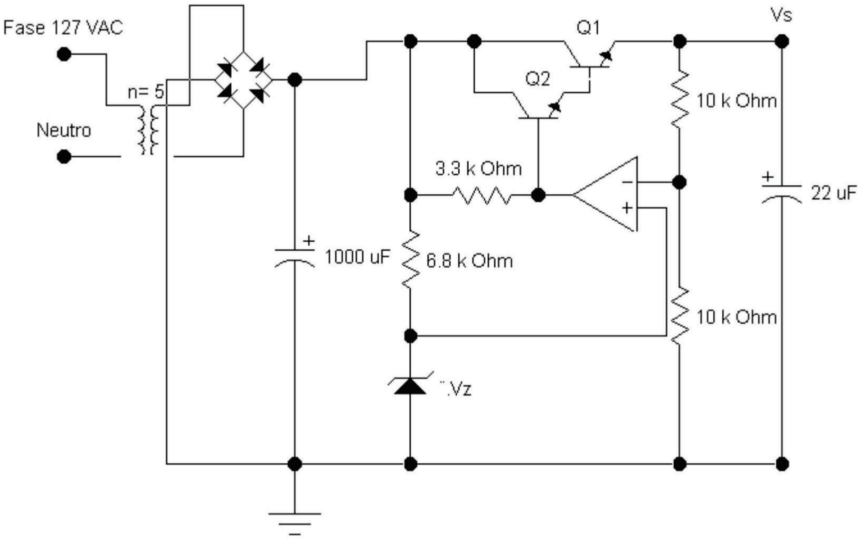
45 - O circuito deste item é usado em instrumentação. Os operacionais são ideais e estão corretamente polarizados.



As tensões V1, V2 e Vs são referidas ao ponto de aterramento. Se a tensão da entrada V1 é igual a tensão da entrada V2, a tensão de saída Vs será igual a:

(A) 200.V1;
(B) 100.V1:
(C) -100.V1;
(D) 50.V1;
(E) zero.

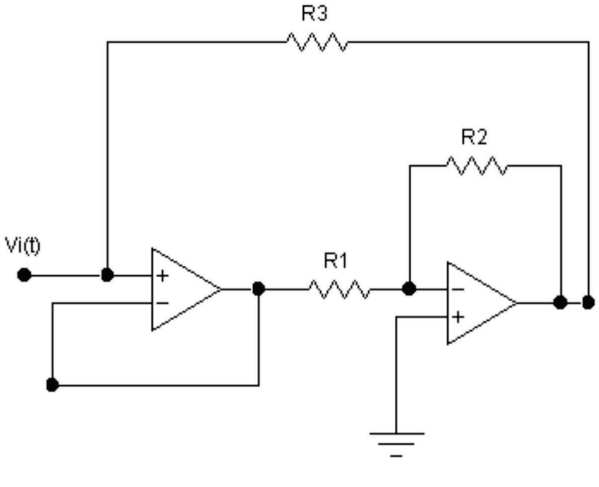
46 - Foi solicitado a um engenheiro que analisasse o circuito abaixo, que é a fonte, que usa regulação série, de um equipamento. A regulação da fonte é feita através dos transistores Q1 e Q2, ambos, de silício. O operacional está perfeitamente polarizado, mas a sua polarização não é mostrada no circuito. O transformador de potência é ligado à rede de 127 VAC e apresenta uma relação de espiras, entre o primário e o secundário (Np/Ns) = n =5, e o diodo Zener tem uma tensão Vz = 9,1 Volts.



Estando o circuito funcionando podemos afirmar que o valor mais próximo da tensão de saída Vs é:

(A) 4,6 Volts;
(B) 9,1 Volts;
(C) 18,2 Volts;
(D) 22,8 Volts;
(E) 34,1 Volts.

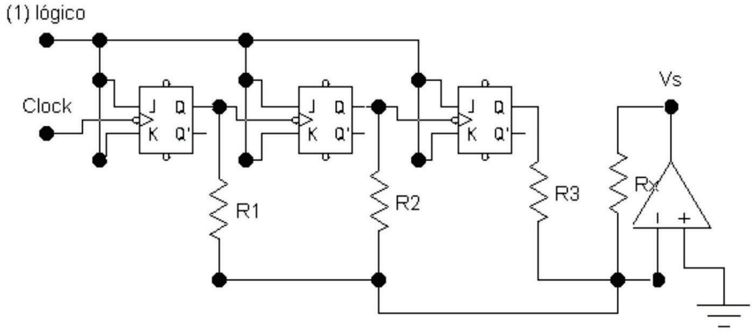
47 - No circuito mostrado neste item os operacionais são ideais, estão corretamente polarizados e os resistores têm valores exatos.



É aplicada na entrada do circuito a tensão Vi(t). Se R1 = 1,0 kΩ, R2 = 9,0 kΩ e R3 = 100 kΩ, a impedância de entrada, [Vi(t)/Ii(t)], sendo Ii(t) a corrente fornecida por Vi(t), é igual a:

(A) 900,0 kΩ;
(B) 100,0 kΩ;
(C) 20,0 kΩ;
(D) 10,0 kΩ;
(E) 1,0 kΩ.

48 - O circuito a seguir é realizado com Flip-flops tipo J-K, estando estas entradas ligadas ao nível (1) lógico. As saídas Q = 12,0 Volts, quando estão no estado (1) lógico, e Q = 0,0 Volts, quando no estado (0) lógico. Os Flip-flops e o operacional, ideais, estão corretamente polarizados. Inicialmente as saídas Q estão em (0) lógico e são comandados pela transição negativa dos pulsos de clock (relógio). As alimentações dos Flip-flops e do operacional não são mostradas

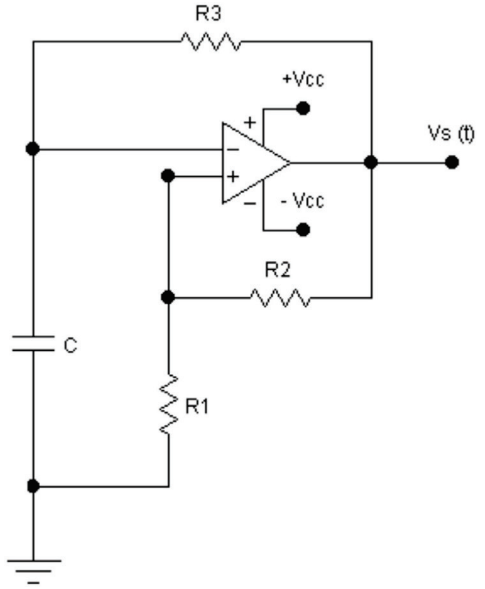


O resistor Rx= 3,0 kΩ. Após 6 (seis) pulsos de clock (relógio) a tensão de saída Vs = – 6,0 Volts. Os valores de R1, R2 e R3 para que isto ocorra são;

(A) R1 = 0,0 kΩ, R2 = 4,0 kΩ e R3 = 2,0 kΩ;
(B) R1 = 30,0 kΩ, R2 = 15,0 kΩ e R3 = 12,0 kΩ;
(C) R1 = 36,0 kΩ, R2 = 18,0 kΩ e R3 = 9,0 kΩ;
(D) R1 = 42,0 kΩ, R2 = 36,0 kΩ e R3 = 18 kΩ;
(E) R1 = 48,0kΩ, R2 = 36,0 kΩ e R3 = 18,0 kΩ.

49 - No circuito apresentado neste item o operacional é ideal e é alimentado com:

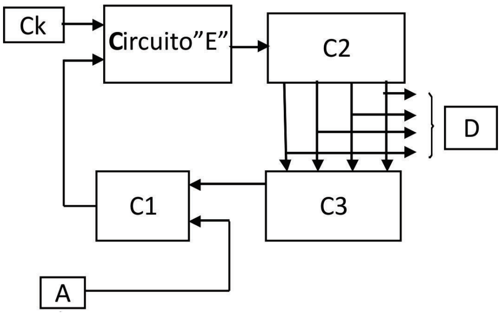
Vcc = +12,0 Volts e - Vcc = -12,0 Volts. Os componentes são exatos e **R2 = 2.R1**.



Podemos afirmar que após o circuito se estabilizar, isto é, no estado permanente, a tensão Vs(t) será uma:

(A) onda triangular com período T = (2/3).R3.C. ln 2/3;
(B) onda quadrada com período T = 2.R3.C.ln 2;
(C) onda com subida e descida exponencial e período T = 0,69.R3.C;
(D) onda com subida e descida exponencial e período T = 12. [R1/(R1+R2)].C;
(E) onda quadrada com período T = 2. [R1.R2)/(R1+R2)]C.ln 2.

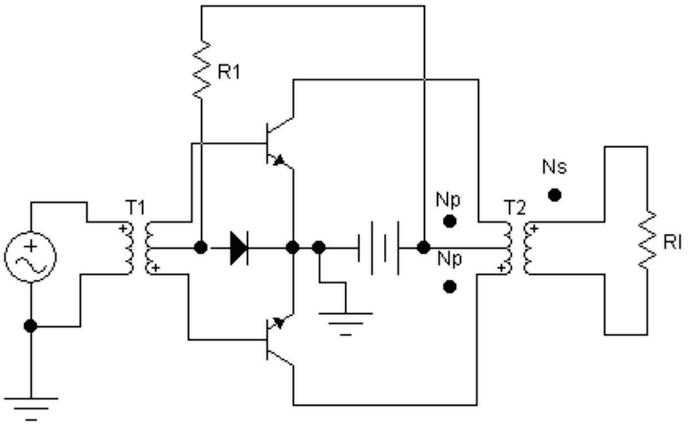
50 - O diagrama em blocos deste item é um diagrama funcional de um Conversor Analógico/Digital (A/D). O terminal "A" é a entrada do sinal analógico, o terminal "Ck" é a entrada de clock (relógio) e os terminais "D" são as saídas digitais. Analise o circuito.



Podemos concluir, que no Conversor A/D mostrado, os circuitos C1, C2 e C3 são:

(A) C1 um Flip-flop R-S, C2 um Integrador e C3 um Contador Johnson;
(B) C1 um Flip-flop J-K, C2 um Contador em Anel e C3 um comparador Diferencial;
(C) C1 um Comparador Diferencial, C2 um Contador BCD e C3 um Conversor Digital/Analógico;
(D) C1 um Flip-flop R-S, C2 um Integrador e C3 um Contador Johnson;
(E) C1 um Comparador Diferencial, C2 um contador em anel e C3 um Conversor Paralelo-Série.

51 - O circuito a seguir é a saída de um amplificador de potência de áudio em classe B Push-Pull, estando os transistores perfeitamente polarizados de modo, inclusive, a não haver distorção de cross-over, e suportando as tensões e correntes do circuito. O transformador de saída (T2) é ideal e tem a relação de espiras (Np/Ns) = 5, sendo Np as espiras de cada metade do primário. Na entrada do amplificador é ligado um gerador de áudio senoidal, com amplitude variável.



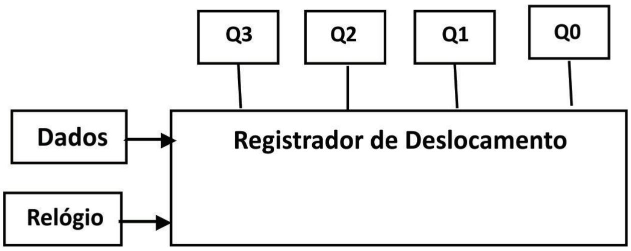
Se a tensão de alimentação é de 12,0 Volts, a tensão de saturação dos transistores é de 2,0 Volts e a resistência de carga Rl = 5,0 Ohms, a potência eficaz máxima na carga, sem distorção, será de aproximadamente:

(A) 100,0 mW;
(B) 400,0 mW;
(C) 6,4 W;
(D) 10,0 W;
(E) 28,8 W.

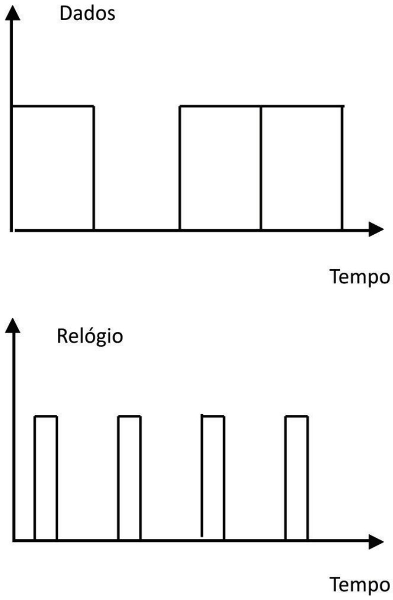
52 - Injetamos um sinal, que fornece uma potência de 10,0 mW, sobre a resistência de entrada de um amplificador de ganho de potência igual a 1000. Na saída, teremos uma potência de:

(A) 50 dBm;
(B) 40 dBm;
(C) 30 dBm;
(D) 20 dBm;
(E) 10 dBm.

53 - O Registrador de Deslocamento, apresentado no diagrama de blocos a seguir, é um circuito lógico sequencial, onde são aplicados dados em série. O Registrador é comandado pela descida do pulso de relógio.



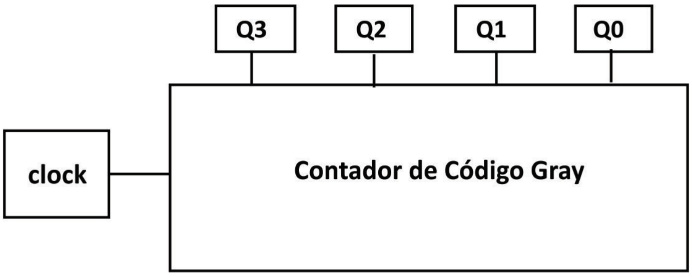
Inicialmente as saídas Q3, Q2, Q1 e Q0 estão em nível "0" lógico. São aplicados, em seguida, os dados em série, D3 = 1, D2 = 0, D1 = 1 e D0 =1, juntamente com os pulsos de relógio, como mostrado no diagrama temporal a seguir.



Após serem aplicados quatro pulsos de relógio teremos nas saídas Q3, Q2, Q1 e Q0:

(A) Q3 = 1 , Q2 = 0, Q1 = 0 e Q0 = 0:
(B) Q3 = 1 , Q2 = 0, Q1 = 0 e Q0 = 1:
(C) Q3 = 1 , Q2 = 0, Q1 = 1 e Q0 = 1:
(D) Q3 = 1 , Q2 = 1, Q1 = 1 e Q0 = 0:
(E) Q3 = 1 , Q2 = 1, Q1 = 1 e Q0 = 1.

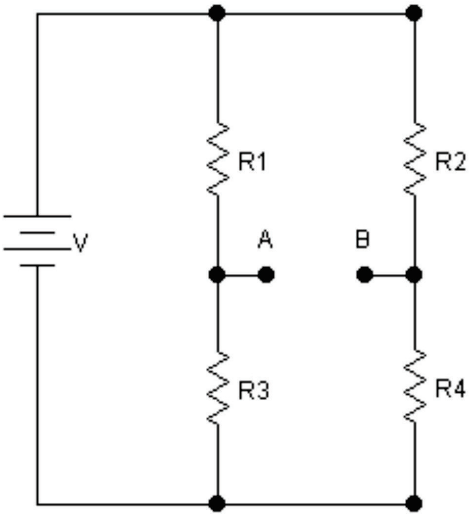
54 -A figura deste item mostra um contador de "Código Gray" de quatro saídas (Q3, Q2, Q1 e Q0), comandados pela descida dos pulsos de um *clock* (relógio). Inicialmente todas as saídas estão em (0) lógico. A saída digital Q3 é a mais significativa.



Após oito pulsos de relógio, teremos Q3, Q2, Q1 e Q0, respectivamente, iguais a:

(A) 1001;
(B) 1100;
(C) 1101;
(D) 1011;
(E) 1111.

55 - Muitas medidas em química e física são feitas usando-se uma ponte de Wheatstone, como a mostrada abaixo.



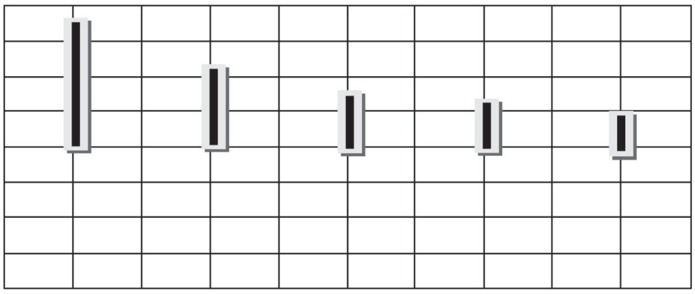
Para qualquer valor da tensão V, a tensão entre o ponto A e o ponto B é igual a zero quando:

(A) R3 = R4;
(B) R1 x R4 = R2 x R3;
(C) R1 x R3 = R2 x R4;
(D) R1 = R2
(E) R1 = R4/R2

56 - Na maioria dos amplificadores é usada uma realimentação negativa, isto é, uma amostragem do sinal de saída, de tensão ou de corrente, é realimentada para a entrada, em série ou em paralelo. Para qualquer topologia de realimentação negativa, podemos afirmar que, em relação ao amplificador original, sem realimentação:

(A) a impedância de entrada aumenta;
(B) a impedância de saída diminui;
(C) o ganho aumenta;
(D) a resposta (banda) de frequência aumenta;
(E) a estabilidade diminui.

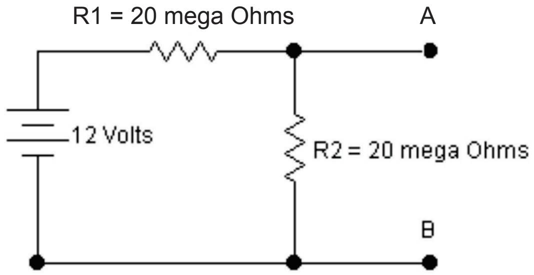
57 - Um analisador de espectro apresenta, em uma tela, os componentes espectrais de um sinal. A figura deste item mostra, de modo estilizado, a tela de um analisador de espectro, onde foi acoplado um sinal na sua entrada para ser analisado. A escala horizontal estava calibrada, em relação à origem, em 10 kHz/divisão.



Concluímos que o sinal de entrada, que mais se aproxima deste espectro, é uma onda:

(A) quadrada de frequência 20 kHz;
(B) quadrada de frequência 10 kHz;
(C) triangular de frequência 5 kHz;
(D) senoidal de frequência 10 kHz, com retificação de meia onda;
(E) senoidal de frequência 20 kHz, com retificação de onda completa.

58 - Um engenheiro quer fazer um voltímetro para medir tensões de zero até 20 VCC, dispondo de um amperímetro que mede no máximo 1,0 μA (micro Amperes) no fundo da escala. Ele construiu o voltímetro, redesenhou a escala em Volts e mediu, com este voltímetro, a tensão entre os pontos "A" e "B" do circuito a seguir.

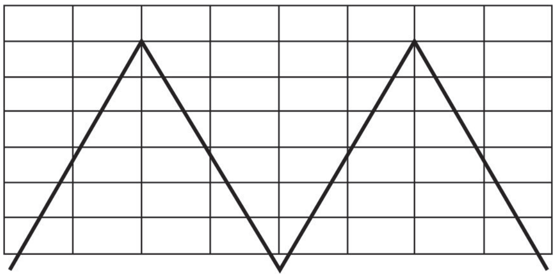


O valor medido foi de:

(A) 2 Volts;
(B) 3 volts;
(C) 4 Volts;
(D) 6 Volts;
(E) 9 Volts.

59 - A figura deste item mostra a tela de um osciloscópio com as seguintes calibrações, respectivamente, na Entrada Vertical e na Base de Tempo:

Entrada Vertical: 2,0 Volts/divisão
Base de Tempo: 2,5 ms/divisão



Podemos concluir pela figura, que na entrada vertical foi acoplado um gerador de sinais triangulares, com uma frequência de aproximadamente:

(A) 10 Hz;
(B) 20 Hz;
(C) 50 Hz;
(D) 100 Hz;
(E) 200 Hz.

60 - Na análise da resposta em frequência de amplificadores, um dos métodos é o Diagrama de Bode, que usa os "pólos" e os "zeros" da função de transferência H(s). É comum fazermos o Diagrama em dois eixos ortogonais, um horizontal e outro vertical. O eixo horizontal graduamos, normalmente, em logaritmo da freqüência (log wi), e o eixo vertical em decibéis do ganho de tensão, isto é, 20 log [A(wi)]. Digamos que a função de transferência apresente os "zeros"

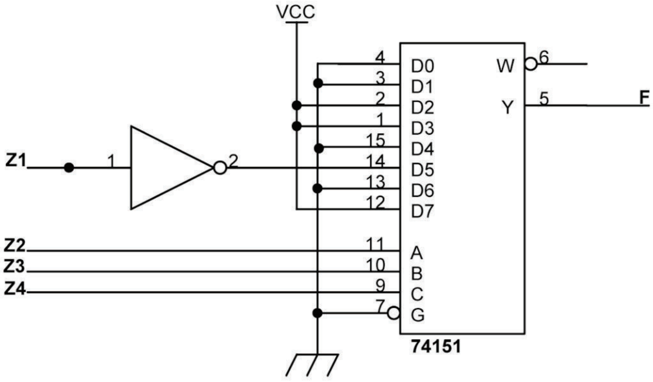
so1, so2... s0n e os "pólos" sp1, sp2... spn.

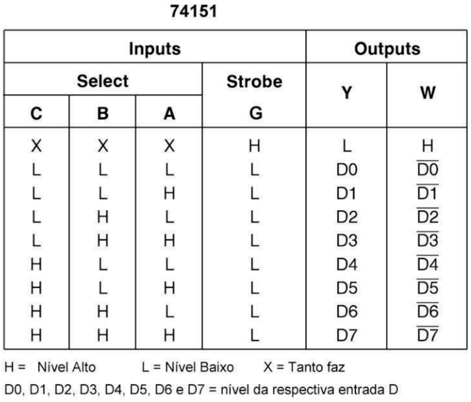
Ao fazermos o Diagrama, quando encontramos um "zero" ou um "pólo, traçamos uma reta de inclinação:

(A) (+6) dB/oitava, quando encontramos um pólo e (– 6 dB)/oitava quando encontramos um zero;
(B) (+20) dB/década, quando encontramos um zero e (–20 dB)/ década quando encontramos um pólo;
(C) (+20) dB/década, quando encontramos um zero e (–20 dB)/ oitava quando encontramos outro zero;
(D) (+ 6) dB/década, quando encontramos um zero e (– 6 dB) /década quando encontramos um pólo;
(E) (+20) dB/oitava, quando encontramos um pólo e (– 20 dB)/ oitava quando encontramos um zero.

61 - Dada a tabela funcional do multiplexador "74151" qual das opções abaixo representa a expressão lógica da saída "F" em função das entradas "Z1", "Z2", "Z3" e "Z4"?

Observação: "x" representa função lógica "AND" e "+" representa a função lógica "OR"




74151

Inputs				Outputs	
Select			Strobe	Y	W
C	B	A	G		
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = Nível Alto L = Nível Baixo X = Tanto faz

D0, D1, D2, D3, D4, D5, D6 e D7 = nível da respectiva entrada D

(A) $F = (Z1 \text{ x } Z3 \text{ x } \overline{Z4}) + (Z2 \text{ x } \overline{Z3} \text{ x } Z4) + (\overline{Z1} \text{ x } Z2 \text{ x } \overline{Z4})$;

(B) $F=(Z1 \text{ x } Z2 \text{ x } Z3) + (Z2 \text{ x } Z4) + (\overline{Z1} \text{ x } Z2 \text{ x } Z3)$;

(C) $F = (\overline{Z2} \text{ x } Z3 \text{ x } Z4) + (\overline{Z1} \text{ x } Z2) + (Z1 \text{ x } Z2 \text{ x } \overline{Z3})$;

(D) $F = (\overline{Z1} \text{ x } Z3) + (\overline{Z2} \text{ x } Z3) + (Z1 \text{ x } \overline{Z2} \text{ x } \overline{Z3} \text{ x } Z4)$;

(E) $F = (Z3 \text{ x } \overline{Z4}) + (Z2 \text{ x } Z3) + (\overline{Z1} \text{ x } Z2 \text{ x } Z4)$.

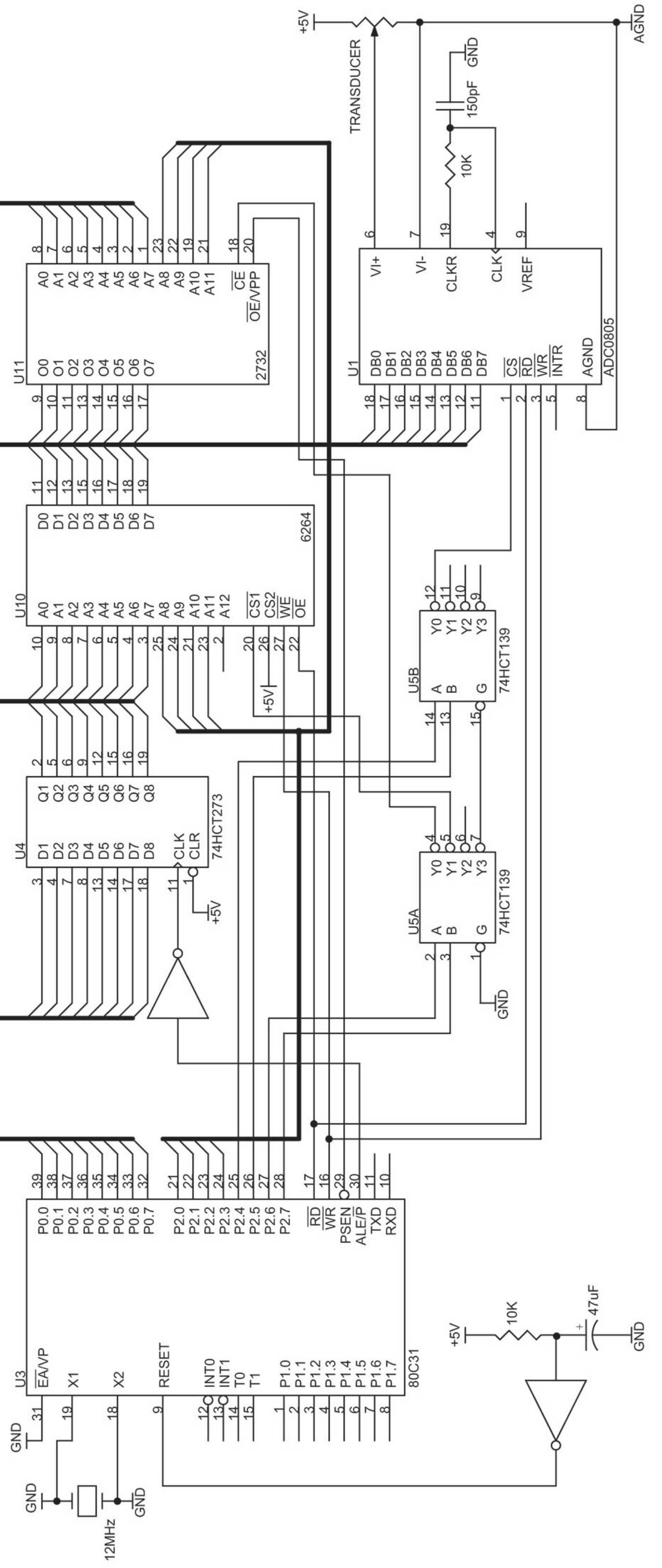
62 - Dado o programa abaixo escrito em linguagem C

```
#include <stdio.h>

        int main()
        {
          int A,B, a,b;

          scanf("%d %d",A,B);
          a = A; b = B;
          while(a!=b) if(a > b) a – = b; else b – = a;
          printf(a);
        }
```

Quando o programa for executado e o operador entrar com os números "16" e "40" qual será o valor que será mostrado na tela como resultado:

(A) 16;
(B) 8;
(C) 0,4;
(D) 2,5;
(E) 40.

O esquema a seguir deve ser utilizado para responder as questões de 63 a 65. Utilize o anexo a esta prova para obter as informações de Manuais Técnicos.



63 - Qual das opções abaixo representa o endereço gerado pelo microcontrolador 80C31(U3) que irá habilitar a leitura do ADC0805 (U1)?

A) $(3000)_{16}$
B) $(2000)_{16}$
C) $(C000)_{16}$
D) $(E000)_{16}$
E) $(F000)_{16}$

64 - Considerando que o byte mais significativo do valor da questão 26 está armazenado na posição (30)16 da memória interna do microcontrolador e que o byte menos significativo do valor da questão 27 está armazenado na posição (31)16 da memória interna do microprocessador, qual dos trechos de programa (em linguagem ASSEMBLY) abaixo implenta a leitura consecutiva de 10 valores digitalizados pelo ADC0805 (U1) e os escreve nas 10 primeiras posições da memória 6264 (U10)?

A)

```
        MOV  DPL,31h
        MOV  DPH,30h
        MOV R0,#10
        MOV R1,#0
LOOP:   MOV A,@DPTR
        NOP
        NOP
        MOV @DPTR,A
        PUSH DPL
        PUSH DPH
        MOV DPH,#0
        MOV DPL, R1
        MOV @DPTR,A
        POP DPH
        POP DPL
        INC R0
        DJNZ R1,LOOP
```

B)

```
        MOV  DPL,31h
        MOV  DPH,30h
        MOV R0,#10
        MOV R1,#0
LOOP:   MOVC A,@A+DPTR
        NOP
        NOP
        MOVX @DPTR,A
        PUSH DPL
        PUSH DPH
        MOV DPH,#0
        MOV DPL, R1
        MOV @DPTR,A
        POP DPH
        POP DPL
        INC R0
        DJNZ R1,LOOP
```

C)

```
        MOV  DPL,31h
        MOV  DPH,30h
        MOV R0,#10
        MOV R1,#0
LOOP:   MOVC A,@A+DPTR
        NOP
        NOP
        MOV @DPTR,A
        PUSH DPL
        PUSH DPH
        MOV DPH,#0
        MOV DPL, R1
        MOV @DPTR,A
        POP DPH
        POP DPL
        INC R0
        DJNZ R1,LOOP
```

D)

```
        MOV  DPL,31h
        MOV  DPH,30h
        MOV R0,#10
        MOV R1,#0
LOOP:   MOVX @DPTR,A
        NOP
        NOP
        MOVC A,@A+DPTR
        MOV DPH,#0
        MOV DPL, R1
        MOV @DPTR,A
        INC R1
        DJNZ R0,LOOP
```

E)

```
        MOV  DPL,31h
        MOV  DPH,30h
        MOV R0,#10
        MOV R1,#0
LOOP:   MOVX @DPTR,A
        NOP
        NOP
        MOVX A,@DPTR
        PUSH DPL
        PUSH DPH
        MOV DPH,#0
        MOV DPL, R1
        MOV @DPTR,A
        POP DPH
        POP DPL
        INC R1
        DJNZ R0,LOOP
```

65 - Se entre os pinos 6 e 7 do ADC0805 (U1) existe uma diferença de potencial de + 3,4 volts qual dos valores abaixo mais se aproxima do valor digitalizado pelo ADC805?

(A) $(10110010)_2$
(B) $(11010001)_2$
(C) $(01011100)_2$
(D) $(10100101)_2$
(E) $(00110101)_2$

ENGENHEIRO ELETRÔNICO

ANEXO

“INFORMAÇÕES DE MANUAIS TÉCNICOS NECESSÁRIAS À SOLUÇÃO DAS QUESTÕES DE 63 A 65”

87C51/80C51BH/80C31BH
CHMOS SINGLE-CHIP 8-BIT MICROCONTROLLER

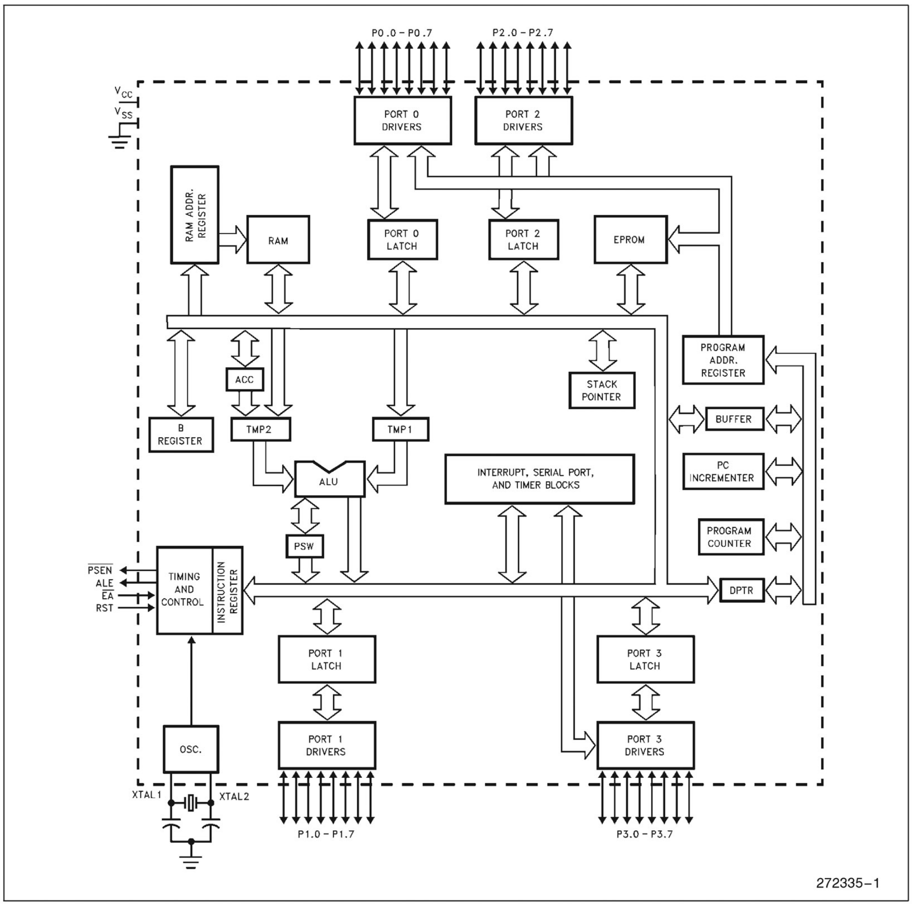
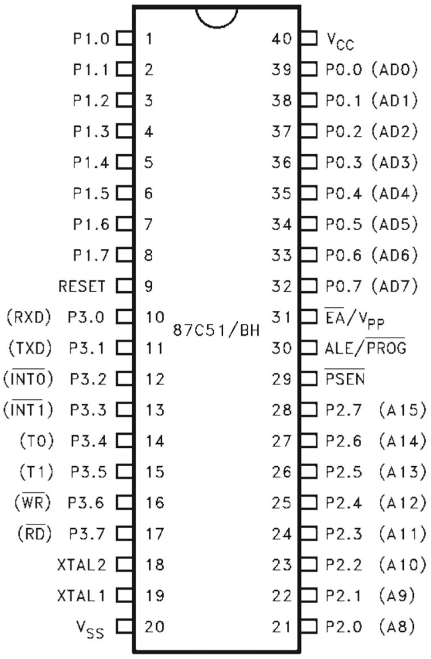


Figure 1. 87C51/BH Block Diagram



PIN DESCRIPTION

V_{CC}: Supply voltage during normal, Idle and Power Down operations.

V_{SS}: Circuit ground.

Port 0: Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink several LS TTL inputs. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external memory. In this application it uses strong internal pullups when emitting 1's.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can drive LS TTL inputs. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program memory and during accesses to external Data Memory that use 16-bit address (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1's.

During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can drive LS TTL inputs. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the MCS-51 Family, as listed below:

RST: Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. The port pins will be driven to their reset condition when a minimum V_{IH1} voltage is applied whether the oscillator is running or not. An internal pulldown resistor permits a power-on reset with only a capacitor connected to V_{CC}.

Pin	Name	Alternate Function
P3.0	RXD	Serial input line
P3.1	TXD	Serial output line
P3.2	$\overline{\text{INT0}}$	External Interrupt 0
P3.3	$\overline{\text{INT1}}$	External Interrupt 1
P3.4	T0	Timer 0 external input
P3.5	T1	Timer 1 external input
P3.6	$\overline{\text{WR}}$	External Data Memory Write strobe
P3.7	$\overline{\text{RD}}$	External Data Memory Read strobe

ALE/$\overline{\text{PROG}}$: Address Latch Enable output signal for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{\text{PROG}}$) during EPROM programming for the 87C51.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With this bit set, the pin is weakly pulled high. However, the ALE disable feature will be suspended during a MOVX or MOVC instruction, idle mode, power down mode and ICE mode. The ALE disable feature will be terminated by reset. When the ALE disable feature is suspended or terminated, the ALE pin will no longer be pulled up weakly. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

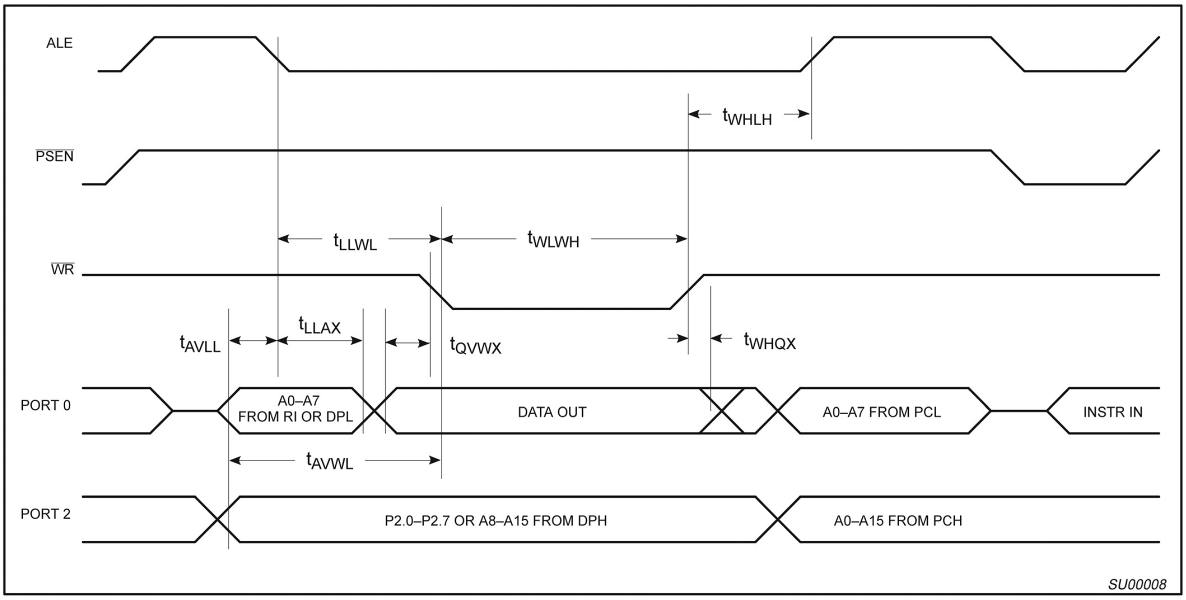
$\overline{\text{PSEN}}$: Program Store Enable is the Read strobe to External Program Memory. When the 87C51/BH is executing from Internal Program Memory, $\overline{\text{PSEN}}$ is inactive (high). When the device is executing code from External Program Memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to External Data Memory.

$\overline{\text{EA}}$/V_{PP}: External Access enable. $\overline{\text{EA}}$ must be strapped to V_{SS} in order to enable the 87C51/BH to fetch code from External Program Memory locations starting at 0000H up to FFFFH. Note, however, that if either of the Lock Bits is programmed, the logic level at $\overline{\text{EA}}$ is internally latched during reset.

$\overline{\text{EA}}$ must be strapped to V_{CC} for internal program execution.

XTAL1: Input to the inverting oscillator amplifier.

XTAL2: Output from the inverting oscillator amplifier.



External Data Memory Write Cycle

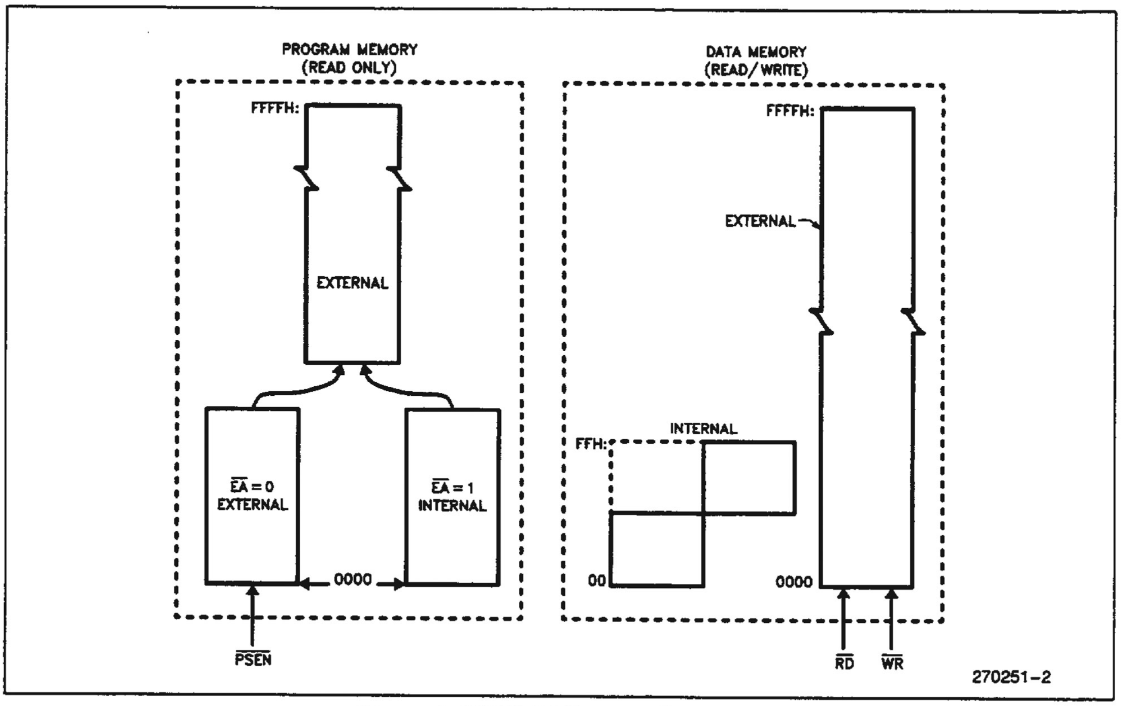


Figure 2. MCS®-51 Memory Structure

CHMOS Devices

Functionally, the CHMOS devices (designated with "C" in the middle of the device name) are all fully compatible with the 8051, but being CMOS, draw less current than an HMOS counterpart. To further exploit the power savings available in CMOS circuitry, two reduced power modes are added:

- Software-invoked Idle Mode, during which the CPU is turned off while the RAM and other on-chip peripherals continue operating. In this mode, current draw is reduced to about 15% of the current drawn when the device is fully active.
- Software-invoked Power Down Mode, during which all on-chip activities are suspended. The on-chip RAM continues to hold its data. In this mode the device typically draws less than 10 μA.

Although the 80C51BH is functionally compatible with its HMOS counterpart, specific differences between the two types of devices must be considered in the design of an application circuit if one wishes to ensure complete interchangeability between the HMOS and CHMOS devices. These considerations are discussed in the Application Note AP-252, "Designing with the 80C51BH".

For more information on the individual devices and features listed in Table 1, refer to the Hardware Descriptions and Data Sheets of the specific device.

MEMORY ORGANIZATION IN MCS®-51 DEVICES

Logical Separation of Program and Data Memory

All MCS-51 devices have separate address spaces for Program and Data Memory, as shown in Figure 2. The logical separation of Program and Data Memory allows the Data Memory to be accessed by 8-bit addresses, which can be more quickly stored and manipulated by an 8-bit CPU. Nevertheless, 16-bit Data Memory addresses can also be generated through the DPTR register.

Program Memory can only be read, not written to. There can be up to 64K bytes of Program Memory. In the ROM and EPROM versions of these devices the lowest 4K, 8K or 16K bytes of Program Memory are provided on-chip. Refer to Table 1 for the amount of on-chip ROM (or EPROM) on each device. In the ROMless versions all Program Memory is external. The read strobe for external Program Memory is the signal $\overline{\text{PSEN}}$ (Program Store Enable).

Data Memory occupies a separate address space from Program Memory. Up to 64K bytes of external RAM can be addressed in the external Data Memory space. The CPU generates read and write signals, $\overline{RD}$ and $\overline{WR}$, as needed during external Data Memory accesses.

External Program Memory and external Data Memory may be combined if desired by applying the $\overline{RD}$ and $\overline{PSEN}$ signals to the inputs of an AND gate and using the output of the gate as the read strobe to the external Program/Data memory.

Program Memory

Figure 3 shows a map of the lower part of the Program Memory. After reset, the CPU begins execution from location 0000H.

As shown in Figure 3, each interrupt is assigned a fixed location in Program Memory. The interrupt causes the CPU to jump to that location, where it commences execution of the service routine. External Interrupt 0, for example, is assigned to location 0003H. If External Interrupt 0 is going to be used, its service routine must begin at location 0003H. If the interrupt is not going to be used, its service location is available as general purpose Program Memory.

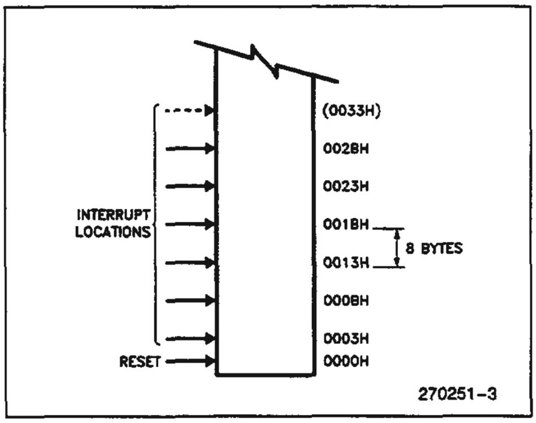


Figure 3. MCS®-51 Program Memory

The interrupt service locations are spaced at 8-byte intervals: 0003H for External Interrupt 0, 000BH for Timer 0, 0013H for External Interrupt 1, 001BH for Timer 1, etc. If an interrupt service routine is short enough (as is often the case in control applications), it can reside entirely within that 8-byte interval. Longer service routines can use a jump instruction to skip over subsequent interrupt locations, if other interrupts are in use.

The lowest 4K (or 8K or 16K) bytes of Program Memory can be either in the on-chip ROM or in an external ROM. This selection is made by strapping the $\overline{EA}$ (External Access) pin to either V_{CC} or V_{SS}.

In the 4K byte ROM devices, if the $\overline{EA}$ pin is strapped to V_{CC}, then program fetches to addresses 0000H through 0FFFH are directed to the internal ROM. Program fetches to addresses 1000H through FFFFH are directed to external ROM.

In the 8K byte ROM devices, $\overline{EA} = V_{CC}$ selects addresses 0000H through 1FFFH to be internal, and addresses 2000H through FFFFH to be external.

In the 16K byte ROM devices, $\overline{EA} = V_{CC}$ selects addresses 0000H through 3FFFH to be internal, and addresses 4000H through FFFFH to be external.

If the $\overline{EA}$ pin is strapped to V_{SS}, then all program fetches are directed to external ROM. The ROMless parts must have this pin externally strapped to V_{SS} to enable them to execute properly.

The read strobe to external ROM, $\overline{PSEN}$, is used for all external program fetches. $\overline{PSEN}$ is not activated for internal program fetches.

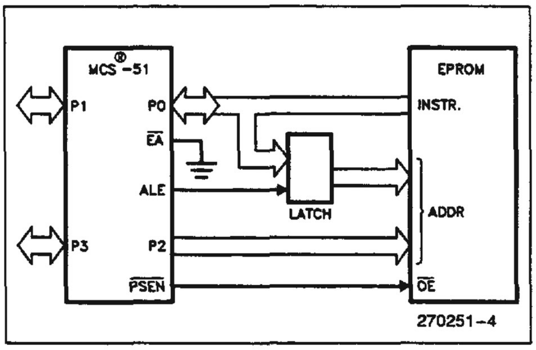


Figure 4. Executing from External Program Memory

The hardware configuration for external program execution is shown in Figure 4. Note that 16 I/O lines (Ports 0 and 2) are dedicated to bus functions during external Program Memory fetches. Port 0 (P0 in Figure 4) serves as a multiplexed address/data bus. It emits the low byte of the Program Counter (PCL) as an address, and then goes into a float state awaiting the arrival of the code byte from the Program Memory. During the time that the low byte of the Program Counter is valid on P0, the signal ALE (Address Latch Enable) clocks this byte into an address latch. Meanwhile, Port 2 (P2 in Figure 4) emits the high byte of the Program Counter (PCH). Then $\overline{PSEN}$ strobes the EPROM and the code byte is read into the microcontroller.

Program Memory addresses are always 16 bits wide, even though the actual amount of Program Memory used may be less than 64K bytes. External program execution sacrifices two of the 8-bit ports, P0 and P2, to the function of addressing the Program Memory.

Data Memory

The right half of Figure 2 shows the internal and external Data Memory spaces available to the MCS-51 user.

Figure 5 shows a hardware configuration for accessing up to 2K bytes of external RAM. The CPU in this case is executing from internal ROM. Port 0 serves as a multiplexed address/data bus to the RAM, and 3 lines of Port 2 are being used to page the RAM. The CPU generates $\overline{RD}$ and $\overline{WR}$ signals as needed during external RAM accesses.

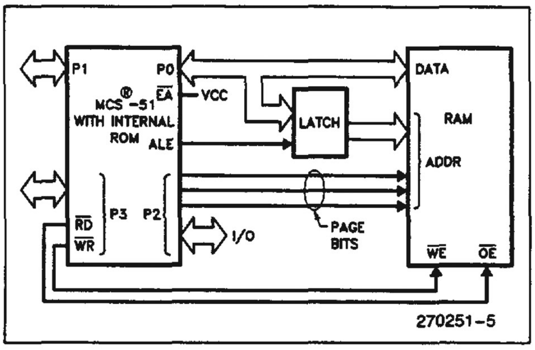


Figure 5. Accessing External Data Memory. If the Program Memory is Internal, the Other Bits of P2 are Available as I/O.

There can be up to 64K bytes of external Data Memory. External Data Memory addresses can be either 1 or 2 bytes wide. One-byte addresses are often used in conjunction with one or more other I/O lines to page the RAM, as shown in Figure 5. Two-byte addresses can also be used, in which case the high address byte is emitted at Port 2.

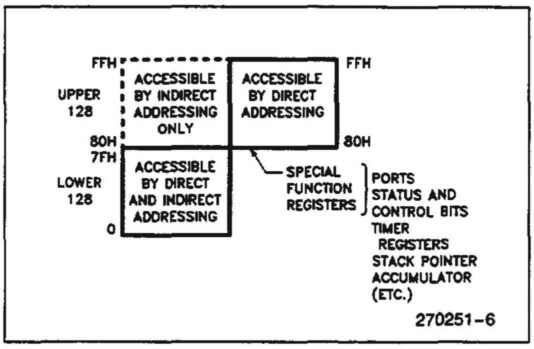


Figure 6. Internal Data Memory

Internal Data Memory is mapped in Figure 6. The memory space is shown divided into three blocks, which are generally referred to as the Lower 128, the Upper 128, and SFR space.

Internal Data Memory addresses are always one byte wide, which implies an address space of only 256 bytes. However, the addressing modes for internal RAM can in fact accommodate 384 bytes, using a simple trick. Direct addresses higher than 7FH access one memory space, and indirect addresses higher than 7FH access a different memory space. Thus Figure 6 shows the Upper 128 and SFR space occupying the same block of addresses, 80H through FFH, although they are physically separate entities.

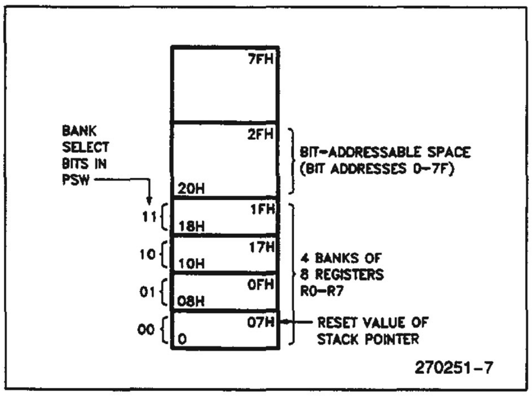


Figure 7. The Lower 128 Bytes of Internal RAM

The Lower 128 bytes of RAM are present in all MCS-51 devices as mapped in Figure 7. The lowest 32 bytes are grouped into 4 banks of 8 registers. Program instructions call out these registers as R0 through R7. Two bits in the Program Status Word (PSW) select which register bank is in use. This allows more efficient use of code space, since register instructions are shorter than instructions that use direct addressing.

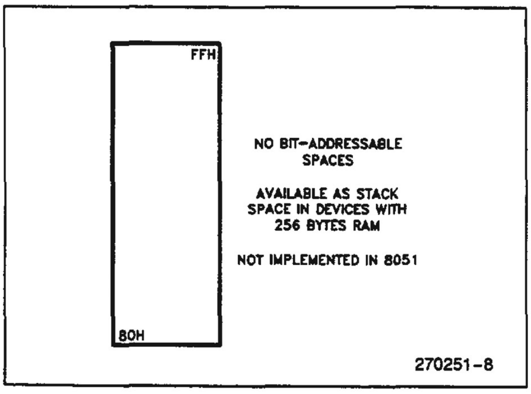


Figure 8. The Upper 128 Bytes of Internal RAM

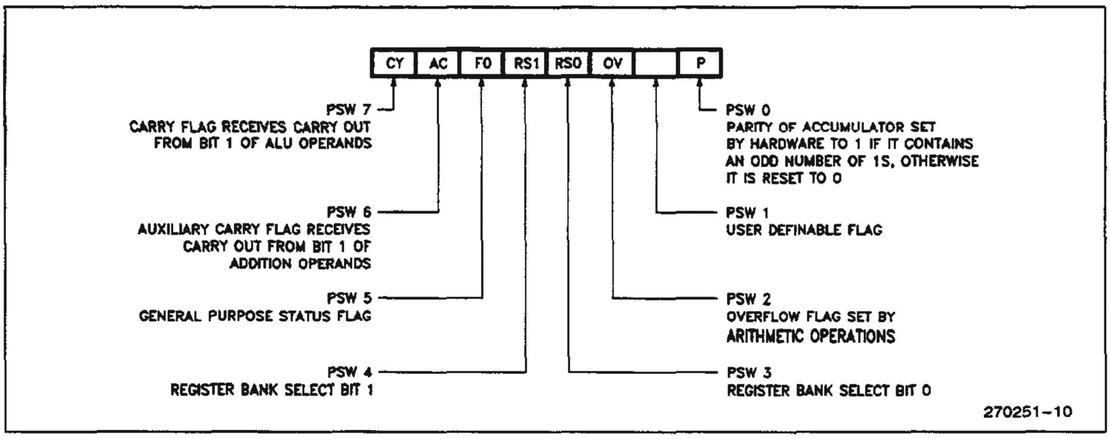

CY
AC
F0
RS1
RS0
OV
P
PSW 7
CARRY FLAG RECEIVES CARRY OUT FROM BIT 1 OF ALU OPERANDS
PSW 6
AUXILIARY CARRY FLAG RECEIVES CARRY OUT FROM BIT 1 OF ADDITION OPERANDS
PSW 5
GENERAL PURPOSE STATUS FLAG
PSW 4
REGISTER BANK SELECT BIT 1
PSW 0
PARITY OF ACCUMULATOR SET BY HARDWARE TO 1 IF IT CONTAINS AN ODD NUMBER OF 1S, OTHERWISE IT IS RESET TO 0
PSW 1
USER DEFINABLE FLAG
PSW 2
OVERFLOW FLAG SET BY ARITHMETIC OPERATIONS
PSW 3
REGISTER BANK SELECT BIT 0
270251-10

Figure 10. PSW (Program Status Word) Register in MCS®-51 Devices

The next 16 bytes above the register banks form a block of bit-addressable memory space. The MCS-51 instruction set includes a wide selection of single-bit instructions, and the 128 bits in this area can be directly addressed by these instructions. The bit addresses in this area are 00H through 7FH.

All of the bytes in the Lower 128 can be accessed by either direct or indirect addressing. The Upper 128 (Figure 8) can only be accessed by indirect addressing. The Upper 128 bytes of RAM are not implemented in the 8051, but are in the devices with 256 bytes of RAM. (See Table 1).

Figure 9 gives a brief look at the Special Function Register (SFR) space. SFRs include the Port latches, timers, peripheral controls, etc. These registers can only be accessed by direct addressing. In general, all MCS-51 microcontrollers have the same SFRs as the 8051, and at the same addresses in SFR space. However, enhancements to the 8051 have additional SFRs that are not present in the 8051, nor perhaps in other proliferations of the family.

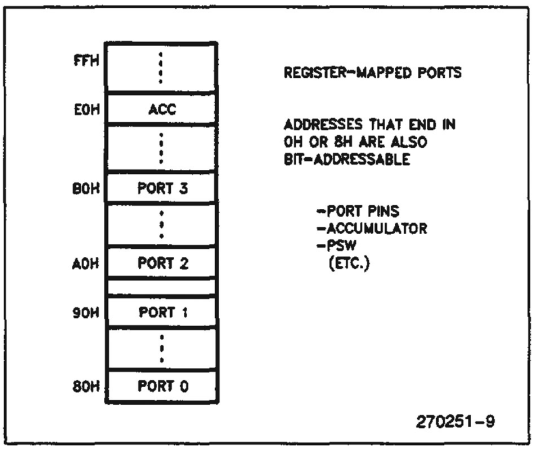


Figure 9. SFR Space

Sixteen addresses in SFR space are both byte- and bit-addressable. The bit-addressable SFRs are those whose address ends in 000B. The bit addresses in this area are 80H through FFH.

THE MCS®-51 INSTRUCTION SET

All members of the MCS-51 family execute the same instruction set. The MCS-51 instruction set is optimized for 8-bit control applications. It provides a variety of fast addressing modes for accessing the internal RAM to facilitate byte operations on small data structures. The instruction set provides extensive support for one-bit variables as a separate data type, allowing direct bit manipulation in control and logic systems that require Boolean processing.

An overview of the MCS-51 instruction set is presented below, with a brief description of how certain instructions might be used. References to "the assembler" in this discussion are to Intel's MCS-51 Macro Assembler, ASM51. More detailed information on the instruction set can be found in the MCS-51 Macro Assembler User's Guide (Order No. 9800937 for ISIS Systems, Order No. 122752 for DOS Systems).

Program Status Word

The Program Status Word (PSW) contains several status bits that reflect the current state of the CPU. The PSW, shown in Figure 10, resides in SFR space. It contains the Carry bit, the Auxiliary Carry (for BCD operations), the two register bank select bits, the Overflow flag, a Parity bit, and two user-definable status flags.

The Carry bit, other than serving the functions of a Carry bit in arithmetic operations, also serves as the "Accumulator" for a number of Boolean operations.

The bits RS0 and RS1 are used to select one of the four register banks shown in Figure 7. A number of instructions refer to these RAM locations as R0 through R7. The selection of which of the four banks is being referred to is made on the basis of the bits RS0 and RS1 at execution time.

The Parity bit reflects the number of 1s in the Accumulator: P = 1 if the Accumulator contains an odd number of 1s, and P = 0 if the Accumulator contains an even number of 1s. Thus the number of 1s in the Accumulator plus P is always even.

Two bits in the PSW are uncommitted and may be used as general purpose status flags.

Addressing Modes

The addressing modes in the MCS-51 instruction set are as follows:

DIRECT ADDRESSING

In direct addressing the operand is specified by an 8-bit address field in the instruction. Only internal Data RAM and SFRs can be directly addressed.

INDIRECT ADDRESSING

In indirect addressing the instruction specifies a register which contains the address of the operand. Both internal and external RAM can be indirectly addressed.

The address register for 8-bit addresses can be R0 or R1 of the selected register bank, or the Stack Pointer. The address register for 16-bit addresses can only be the 16-bit "data pointer" register, DPTR.

REGISTER INSTRUCTIONS

The register banks, containing registers R0 through R7, can be accessed by certain instructions which carry a 3-bit register specification within the opcode of the instruction. Instructions that access the registers this way are code efficient, since this mode eliminates an address byte. When the instruction is executed, one of the eight registers in the selected bank is accessed. One of four banks is selected at execution time by the two bank select bits in the PSW.

REGISTER-SPECIFIC INSTRUCTIONS

Some instructions are specific to a certain register. For example, some instructions always operate on the Accumulator, or Data Pointer, etc., so no address byte is needed to point to it. The opcode itself does that. Instructions that refer to the Accumlator as A assemble as accumulator-specific opcodes.

IMMEDIATE CONSTANTS

The value of a constant can follow the opcode in Program Memory. For example,

```
MOV A, #100
```

loads the Accumulator with the decimal number 100. The same number could be specified in hex digits as 64H.

INDEXED ADDRESSING

Only Program Memory can be accessed with indexed addressing, and it can only be read. This addressing mode is intended for reading look-up tables in Program Memory. A 16-bit base register (either DPTR or the Program Counter) points to the base of the table, and the Accumulator is set up with the table entry number. The address of the table entry in Program Memory is formed by adding the Accumulator data to the base pointer.

Another type of indexed addressing is used in the "case jump" instruction. In this case the destination address of a jump instruction is computed as the sum of the base pointer and the Accumulator data.

Arithmetic Instructions

The menu of arithmetic instructions is listed in Table 2. The table indicates the addressing modes that can be used with each instruction to access the <byte> operand. For example, the ADD A,<byte> instruction can be written as:

```
ADD    A,7FH     (direct addressing)
ADD    A,@R0     (indirect addressing)
ADD    A,R7      (register addressing)
ADD    A,#127    (immediate constant)
```

The execution times listed in Table 2 assume a 12 MHz clock frequency. All of the arithmetic instructions execute in 1 μs except the INC DPTR instruction, which takes 2 μs, and the Multiply and Divide instructions, which take 4 μs.

Note that any byte in the internal Data Memory space can be incremented or decremented without going through the Accumulator.

One of the INC instructions operates on the 16-bit Data Pointer. The Data Pointer is used to generate 16-bit addresses for external memory, so being able to increment it in one 16-bit operation is a useful feature.

The MUL AB instruction multiplies the Accumulator by the data in the B register and puts the 16-bit product into the concatenated B and Accumulator registers.

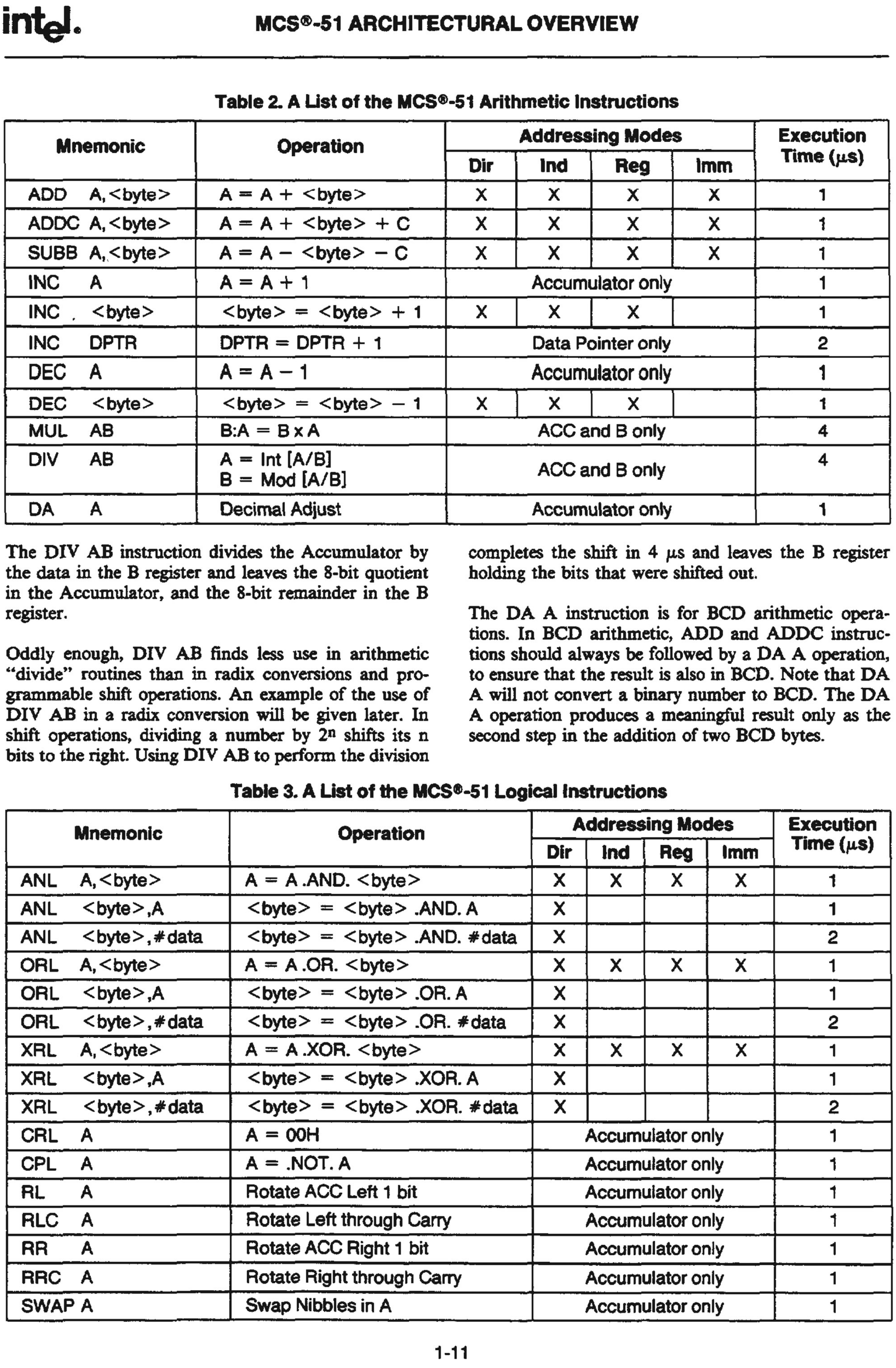


Table 2. A List of the MCS®-51 Arithmetic Instructions

Mnemonic	Operation	Addressing Modes				Execution Time (μs)
		Dir	Ind	Reg	Imm	
ADD A,<byte>	A = A + <byte>	X	X	X	X	1
ADDC A,<byte>	A = A + <byte> + C	X	X	X	X	1
SUBB A,<byte>	A = A − <byte> − C	X	X	X	X	1
INC A	A = A + 1	Accumulator only				1
INC <byte>	<byte> = <byte> + 1	X	X	X		1
INC DPTR	DPTR = DPTR + 1	Data Pointer only				2
DEC A	A = A − 1	Accumulator only				1
DEC <byte>	<byte> = <byte> − 1	X	X	X		1
MUL AB	B:A = B x A	ACC and B only				4
DIV AB	A = Int [A/B] B = Mod [A/B]	ACC and B only				4
DA A	Decimal Adjust	Accumulator only				1

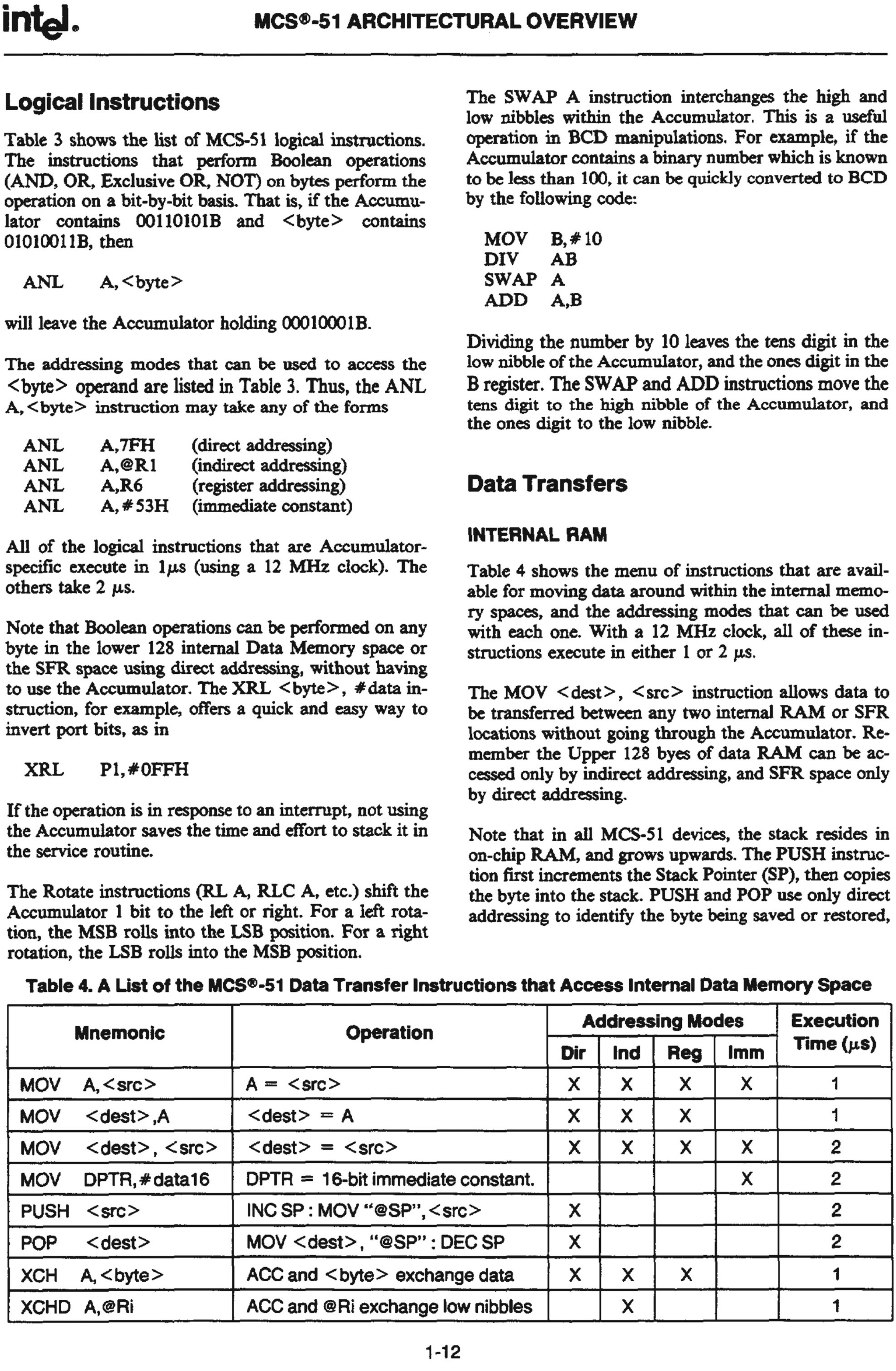
The DIV AB instruction divides the Accumulator by the data in the B register and leaves the 8-bit quotient in the Accumulator, and the 8-bit remainder in the B register.

Oddly enough, DIV AB finds less use in arithmetic "divide" routines than in radix conversions and programmable shift operations. An example of the use of DIV AB in a radix conversion will be given later. In shift operations, dividing a number by 2^n shifts its n bits to the right. Using DIV AB to perform the division completes the shift in 4 μs and leaves the B register holding the bits that were shifted out.

The DA A instruction is for BCD arithmetic operations. In BCD arithmetic, ADD and ADDC instructions should always be followed by a DA A operation, to ensure that the result is also in BCD. Note that DA A will not convert a binary number to BCD. The DA A operation produces a meaningful result only as the second step in the addition of two BCD bytes.

Table 3. A List of the MCS®-51 Logical Instructions

Mnemonic	Operation	Addressing Modes				Execution Time (μs)
		Dir	Ind	Reg	Imm	
ANL A,<byte>	A = A .AND. <byte>	X	X	X	X	1
ANL <byte>,A	<byte> = <byte> .AND. A	X				1
ANL <byte>,#data	<byte> = <byte> .AND. #data	X				2
ORL A,<byte>	A = A .OR. <byte>	X	X	X	X	1
ORL <byte>,A	<byte> = <byte> .OR. A	X				1
ORL <byte>,#data	<byte> = <byte> .OR. #data	X				2
XRL A,<byte>	A = A .XOR. <byte>	X	X	X	X	1
XRL <byte>,A	<byte> = <byte> .XOR. A	X				1
XRL <byte>,#data	<byte> = <byte> .XOR. #data	X				2
CRL A	A = 00H	Accumulator only				1
CPL A	A = .NOT. A	Accumulator only				1
RL A	Rotate ACC Left 1 bit	Accumulator only				1
RLC A	Rotate Left through Carry	Accumulator only				1
RR A	Rotate ACC Right 1 bit	Accumulator only				1
RRC A	Rotate Right through Carry	Accumulator only				1
SWAP A	Swap Nibbles in A	Accumulator only				1



Logical Instructions

Table 3 shows the list of MCS-51 logical instructions. The instructions that perform Boolean operations (AND, OR, Exclusive OR, NOT) on bytes perform the operation on a bit-by-bit basis. That is, if the Accumulator contains 00110101B and <byte> contains 01010011B, then

```
ANL     A,<byte>
```

will leave the Accumulator holding 00010001B.

The addressing modes that can be used to access the <byte> operand are listed in Table 3. Thus, the ANL A,<byte> instruction may take any of the forms

```
ANL     A,7FH     (direct addressing)
ANL     A,@R1     (indirect addressing)
ANL     A,R6      (register addressing)
ANL     A,#53H    (immediate constant)
```

All of the logical instructions that are Accumulator-specific execute in 1μs (using a 12 MHz clock). The others take 2 μs.

Note that Boolean operations can be performed on any byte in the lower 128 internal Data Memory space or the SFR space using direct addressing, without having to use the Accumulator. The XRL <byte>, #data instruction, for example, offers a quick and easy way to invert port bits, as in

```
XRL     P1,#0FFH
```

If the operation is in response to an interrupt, not using the Accumulator saves the time and effort to stack it in the service routine.

The Rotate instructions (RL A, RLC A, etc.) shift the Accumulator 1 bit to the left or right. For a left rotation, the MSB rolls into the LSB position. For a right rotation, the LSB rolls into the MSB position.

The SWAP A instruction interchanges the high and low nibbles within the Accumulator. This is a useful operation in BCD manipulations. For example, if the Accumulator contains a binary number which is known to be less than 100, it can be quickly converted to BCD by the following code:

```
MOV   B,#10
DIV   AB
SWAP  A
ADD   A,B
```

Dividing the number by 10 leaves the tens digit in the low nibble of the Accumulator, and the ones digit in the B register. The SWAP and ADD instructions move the tens digit to the high nibble of the Accumulator, and the ones digit to the low nibble.

Data Transfers

INTERNAL RAM

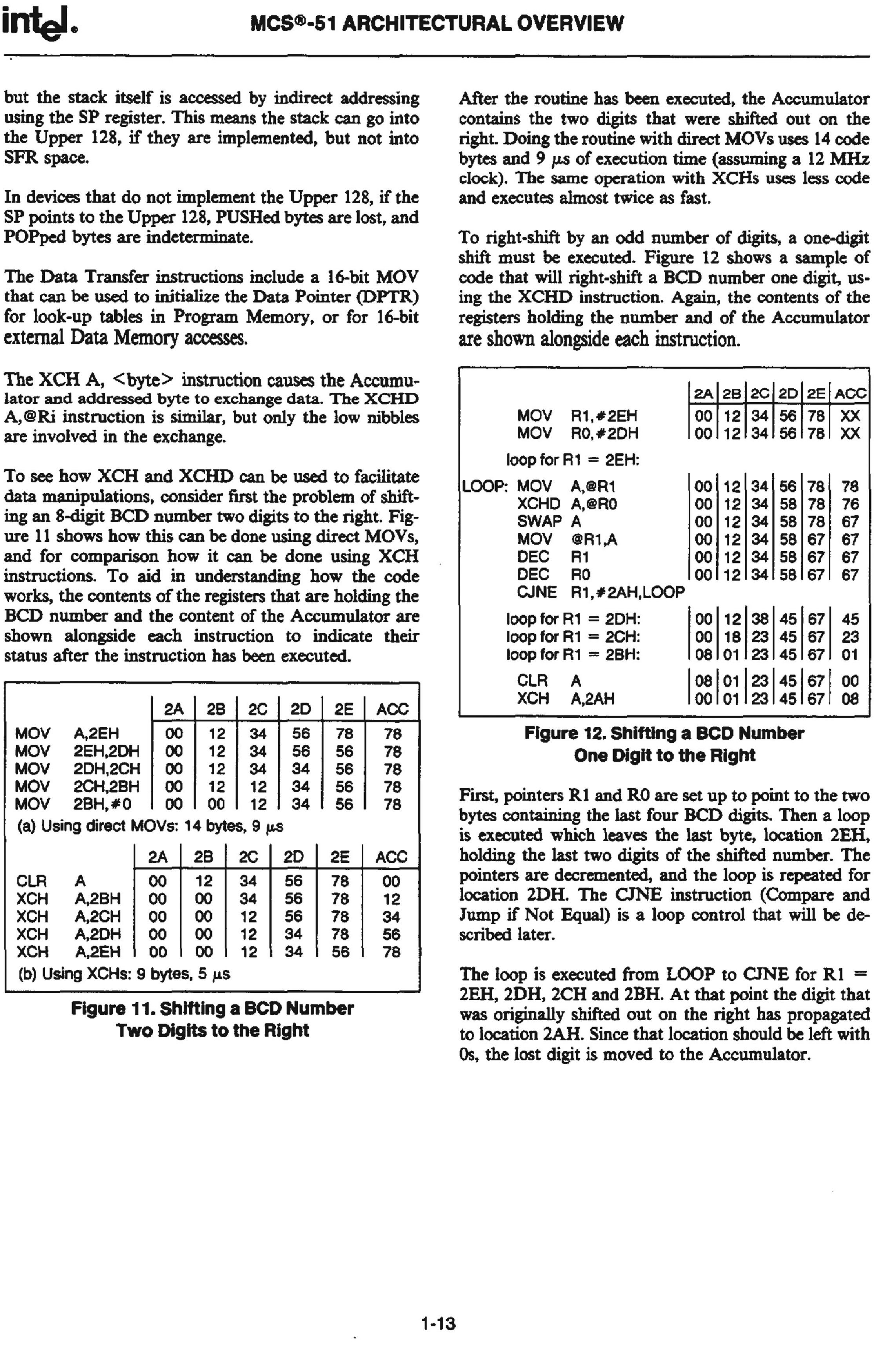
Table 4 shows the menu of instructions that are available for moving data around within the internal memory spaces, and the addressing modes that can be used with each one. With a 12 MHz clock, all of these instructions execute in either 1 or 2 μs.

The MOV <dest>, <src> instruction allows data to be transferred between any two internal RAM or SFR locations without going through the Accumulator. Remember the Upper 128 byes of data RAM can be accessed only by indirect addressing, and SFR space only by direct addressing.

Note that in all MCS-51 devices, the stack resides in on-chip RAM, and grows upwards. The PUSH instruction first increments the Stack Pointer (SP), then copies the byte into the stack. PUSH and POP use only direct addressing to identify the byte being saved or restored,

Table 4. A List of the MCS®-51 Data Transfer Instructions that Access Internal Data Memory Space

Mnemonic	Operation	Addressing Modes				Execution Time (μs)
		Dir	Ind	Reg	Imm	
MOV A,<src>	A = <src>	X	X	X	X	1
MOV <dest>,A	<dest> = A	X	X	X		1
MOV <dest>, <src>	<dest> = <src>	X	X	X	X	2
MOV DPTR,#data16	DPTR = 16-bit immediate constant.				X	2
PUSH <src>	INC SP : MOV "@SP",<src>	X				2
POP <dest>	MOV <dest>, "@SP" : DEC SP	X				2
XCH A,<byte>	ACC and <byte> exchange data	X	X	X		1
XCHD A,@Ri	ACC and @Ri exchange low nibbles		X			1



but the stack itself is accessed by indirect addressing using the SP register. This means the stack can go into the Upper 128, if they are implemented, but not into SFR space.

In devices that do not implement the Upper 128, if the SP points to the Upper 128, PUSHed bytes are lost, and POPped bytes are indeterminate.

The Data Transfer instructions include a 16-bit MOV that can be used to initialize the Data Pointer (DPTR) for look-up tables in Program Memory, or for 16-bit external Data Memory accesses.

The XCH A, <byte> instruction causes the Accumulator and addressed byte to exchange data. The XCHD A,@Ri instruction is similar, but only the low nibbles are involved in the exchange.

To see how XCH and XCHD can be used to facilitate data manipulations, consider first the problem of shifting an 8-digit BCD number two digits to the right. Figure 11 shows how this can be done using direct MOVs, and for comparison how it can be done using XCH instructions. To aid in understanding how the code works, the contents of the registers that are holding the BCD number and the content of the Accumulator are shown alongside each instruction to indicate their status after the instruction has been executed.

		2A	2B	2C	2D	2E	ACC
MOV	A,2EH	00	12	34	56	78	78
MOV	2EH,2DH	00	12	34	56	56	78
MOV	2DH,2CH	00	12	34	34	56	78
MOV	2CH,2BH	00	12	12	34	56	78
MOV	2BH,#0	00	00	12	34	56	78

(a) Using direct MOVs: 14 bytes, 9 μs

		2A	2B	2C	2D	2E	ACC
CLR	A	00	12	34	56	78	00
XCH	A,2BH	00	00	34	56	78	12
XCH	A,2CH	00	00	12	56	78	34
XCH	A,2DH	00	00	12	34	78	56
XCH	A,2EH	00	00	12	34	56	78

(b) Using XCHs: 9 bytes, 5 μs

Figure 11. Shifting a BCD Number Two Digits to the Right

After the routine has been executed, the Accumulator contains the two digits that were shifted out on the right. Doing the routine with direct MOVs uses 14 code bytes and 9 μs of execution time (assuming a 12 MHz clock). The same operation with XCHs uses less code and executes almost twice as fast.

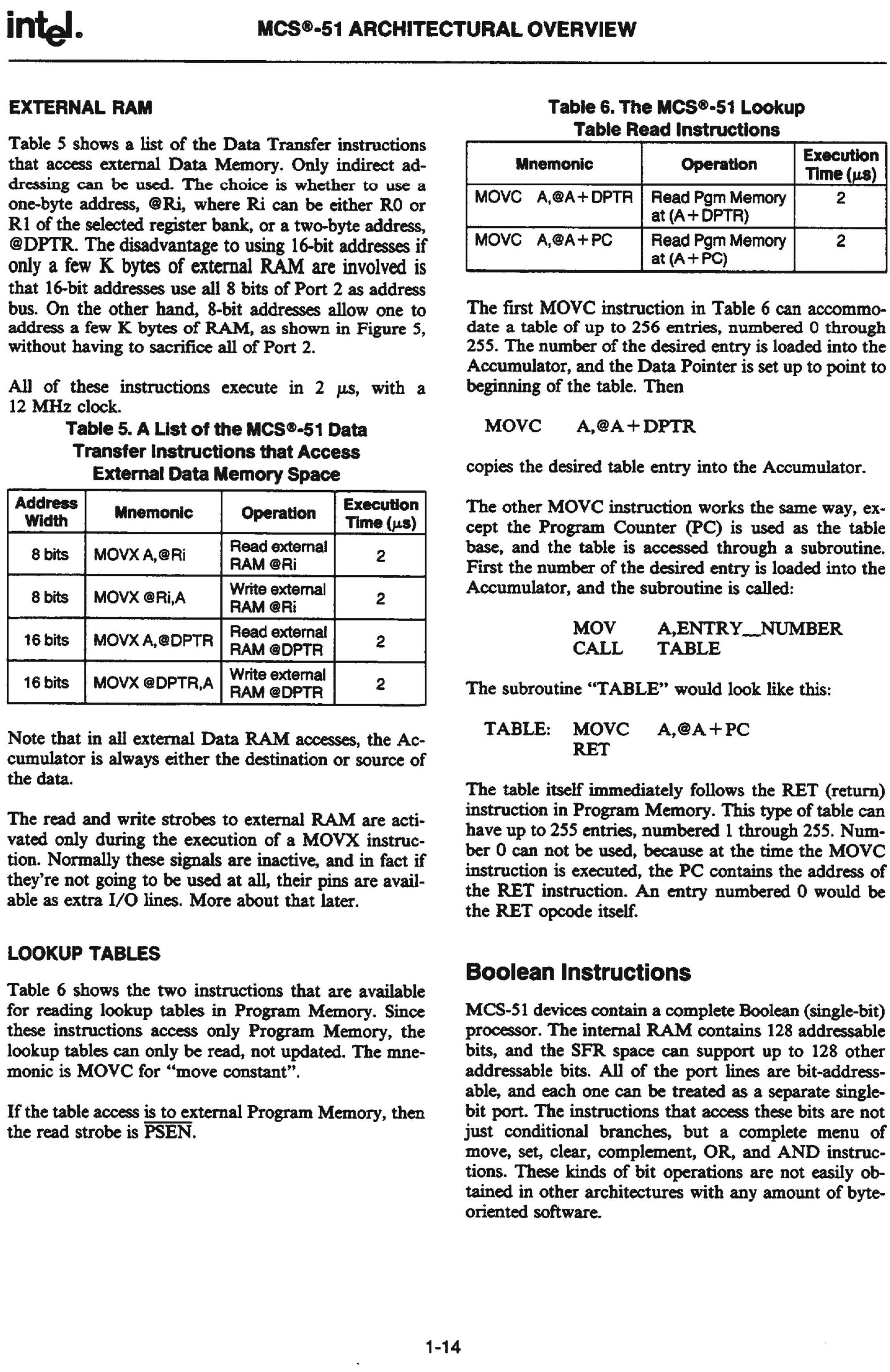
To right-shift by an odd number of digits, a one-digit shift must be executed. Figure 12 shows a sample of code that will right-shift a BCD number one digit, using the XCHD instruction. Again, the contents of the registers holding the number and of the Accumulator are shown alongside each instruction.

			2A	2B	2C	2D	2E	ACC
	MOV	R1,#2EH	00	12	34	56	78	XX
	MOV	R0,#2DH	00	12	34	56	78	XX
	loop for R1 = 2EH:							
LOOP:	MOV	A,@R1	00	12	34	56	78	78
	XCHD	A,@R0	00	12	34	58	78	76
	SWAP	A	00	12	34	58	78	67
	MOV	@R1,A	00	12	34	58	67	67
	DEC	R1	00	12	34	58	67	67
	DEC	R0	00	12	34	58	67	67
	CJNE	R1,#2AH,LOOP						
	loop for R1 = 2DH:		00	12	38	45	67	45
	loop for R1 = 2CH:		00	18	23	45	67	23
	loop for R1 = 2BH:		08	01	23	45	67	01
	CLR	A	08	01	23	45	67	00
	XCH	A,2AH	00	01	23	45	67	08

Figure 12. Shifting a BCD Number One Digit to the Right

First, pointers R1 and R0 are set up to point to the two bytes containing the last four BCD digits. Then a loop is executed which leaves the last byte, location 2EH, holding the last two digits of the shifted number. The pointers are decremented, and the loop is repeated for location 2DH. The CJNE instruction (Compare and Jump if Not Equal) is a loop control that will be described later.

The loop is executed from LOOP to CJNE for R1 = 2EH, 2DH, 2CH and 2BH. At that point the digit that was originally shifted out on the right has propagated to location 2AH. Since that location should be left with 0s, the lost digit is moved to the Accumulator.



EXTERNAL RAM

Table 5 shows a list of the Data Transfer instructions that access external Data Memory. Only indirect addressing can be used. The choice is whether to use a one-byte address, @Ri, where Ri can be either R0 or R1 of the selected register bank, or a two-byte address, @DPTR. The disadvantage to using 16-bit addresses if only a few K bytes of external RAM are involved is that 16-bit addresses use all 8 bits of Port 2 as address bus. On the other hand, 8-bit addresses allow one to address a few K bytes of RAM, as shown in Figure 5, without having to sacrifice all of Port 2.

All of these instructions execute in 2 μs, with a 12 MHz clock.

Table 5. A List of the MCS®-51 Data Transfer Instructions that Access External Data Memory Space

Address Width	Mnemonic	Operation	Execution Time (μs)
8 bits	MOVX A,@Ri	Read external RAM @Ri	2
8 bits	MOVX @Ri,A	Write external RAM @Ri	2
16 bits	MOVX A,@DPTR	Read external RAM @DPTR	2
16 bits	MOVX @DPTR,A	Write external RAM @DPTR	2

Note that in all external Data RAM accesses, the Accumulator is always either the destination or source of the data.

The read and write strobes to external RAM are activated only during the execution of a MOVX instruction. Normally these signals are inactive, and in fact if they're not going to be used at all, their pins are available as extra I/O lines. More about that later.

LOOKUP TABLES

Table 6 shows the two instructions that are available for reading lookup tables in Program Memory. Since these instructions access only Program Memory, the lookup tables can only be read, not updated. The mnemonic is MOVC for "move constant".

If the table access is to external Program Memory, then the read strobe is $\overline{\text{PSEN}}$.

Table 6. The MCS®-51 Lookup Table Read Instructions

Mnemonic	Operation	Execution Time (μs)
MOVC A,@A+DPTR	Read Pgm Memory at (A+DPTR)	2
MOVC A,@A+PC	Read Pgm Memory at (A+PC)	2

The first MOVC instruction in Table 6 can accommodate a table of up to 256 entries, numbered 0 through 255. The number of the desired entry is loaded into the Accumulator, and the Data Pointer is set up to point to beginning of the table. Then

```
MOVC    A,@A+DPTR
```

copies the desired table entry into the Accumulator.

The other MOVC instruction works the same way, except the Program Counter (PC) is used as the table base, and the table is accessed through a subroutine. First the number of the desired entry is loaded into the Accumulator, and the subroutine is called:

```
         MOV     A,ENTRY_NUMBER
         CALL    TABLE
```

The subroutine "TABLE" would look like this:

```
TABLE:   MOVC    A,@A+PC
         RET
```

The table itself immediately follows the RET (return) instruction in Program Memory. This type of table can have up to 255 entries, numbered 1 through 255. Number 0 can not be used, because at the time the MOVC instruction is executed, the PC contains the address of the RET instruction. An entry numbered 0 would be the RET opcode itself.

Boolean Instructions

MCS-51 devices contain a complete Boolean (single-bit) processor. The internal RAM contains 128 addressable bits, and the SFR space can support up to 128 other addressable bits. All of the port lines are bit-addressable, and each one can be treated as a separate single-bit port. The instructions that access these bits are not just conditional branches, but a complete menu of move, set, clear, complement, OR, and AND instructions. These kinds of bit operations are not easily obtained in other architectures with any amount of byte-oriented software.

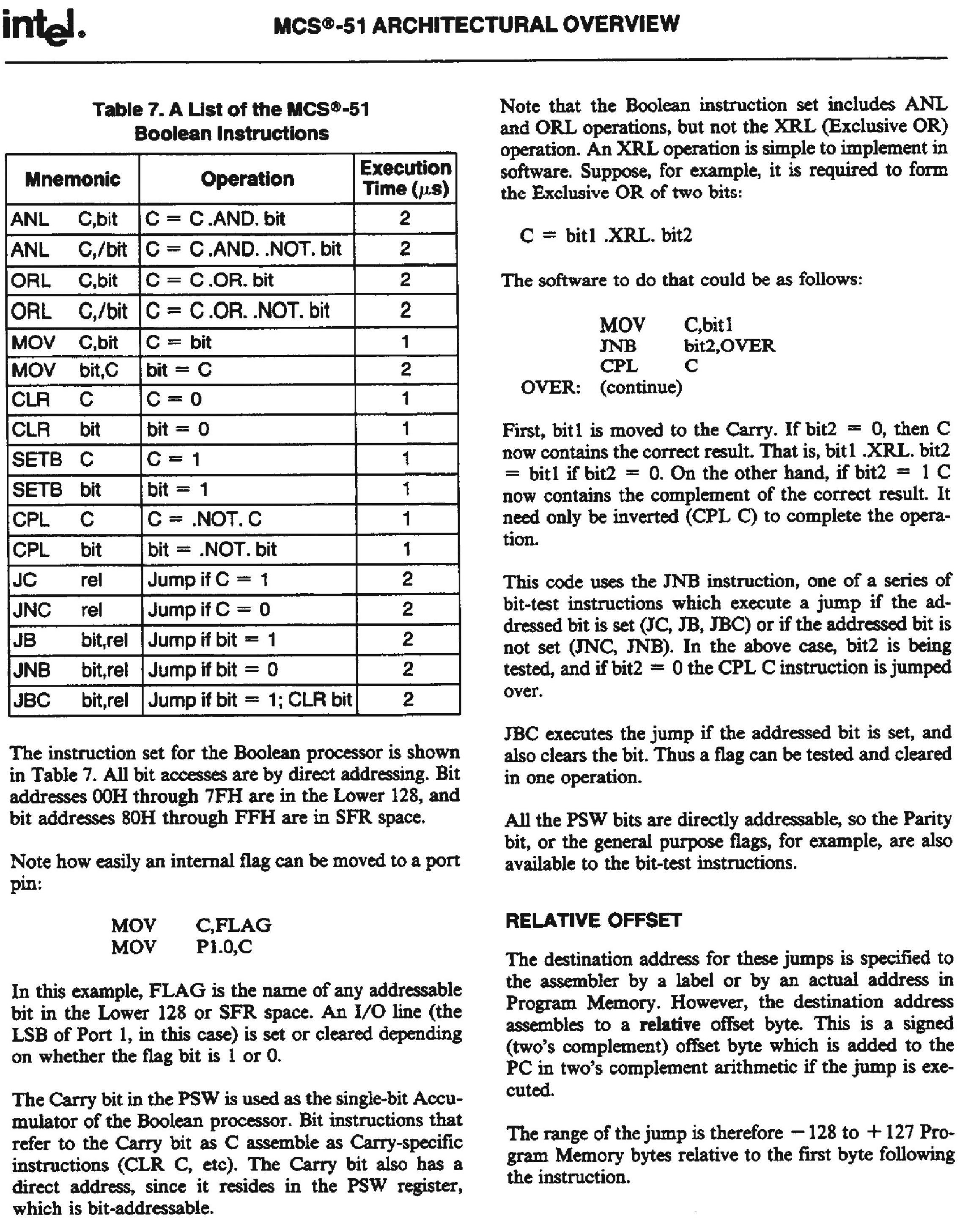


Table 7. A List of the MCS®-51 Boolean Instructions

Mnemonic		Operation	Execution Time (μs)
ANL	C,bit	C = C .AND. bit	2
ANL	C,/bit	C = C .AND. .NOT. bit	2
ORL	C,bit	C = C .OR. bit	2
ORL	C,/bit	C = C .OR. .NOT. bit	2
MOV	C,bit	C = bit	1
MOV	bit,C	bit = C	2
CLR	C	C = 0	1
CLR	bit	bit = 0	1
SETB	C	C = 1	1
SETB	bit	bit = 1	1
CPL	C	C = .NOT. C	1
CPL	bit	bit = .NOT. bit	1
JC	rel	Jump if C = 1	2
JNC	rel	Jump if C = 0	2
JB	bit,rel	Jump if bit = 1	2
JNB	bit,rel	Jump if bit = 0	2
JBC	bit,rel	Jump if bit = 1; CLR bit	2

The instruction set for the Boolean processor is shown in Table 7. All bit accesses are by direct addressing. Bit addresses 00H through 7FH are in the Lower 128, and bit addresses 80H through FFH are in SFR space.

Note how easily an internal flag can be moved to a port pin:

```
MOV     C,FLAG
MOV     P1.0,C
```

In this example, FLAG is the name of any addressable bit in the Lower 128 or SFR space. An I/O line (the LSB of Port 1, in this case) is set or cleared depending on whether the flag bit is 1 or 0.

The Carry bit in the PSW is used as the single-bit Accumulator of the Boolean processor. Bit instructions that refer to the Carry bit as C assemble as Carry-specific instructions (CLR C, etc). The Carry bit also has a direct address, since it resides in the PSW register, which is bit-addressable.

Note that the Boolean instruction set includes ANL and ORL operations, but not the XRL (Exclusive OR) operation. An XRL operation is simple to implement in software. Suppose, for example, it is required to form the Exclusive OR of two bits:

C = bit1 .XRL. bit2

The software to do that could be as follows:

```
        MOV     C,bit1
        JNB     bit2,OVER
        CPL     C
OVER:   (continue)
```

First, bit1 is moved to the Carry. If bit2 = 0, then C now contains the correct result. That is, bit1 .XRL. bit2 = bit1 if bit2 = 0. On the other hand, if bit2 = 1 C now contains the complement of the correct result. It need only be inverted (CPL C) to complete the operation.

This code uses the JNB instruction, one of a series of bit-test instructions which execute a jump if the addressed bit is set (JC, JB, JBC) or if the addressed bit is not set (JNC, JNB). In the above case, bit2 is being tested, and if bit2 = 0 the CPL C instruction is jumped over.

JBC executes the jump if the addressed bit is set, and also clears the bit. Thus a flag can be tested and cleared in one operation.

All the PSW bits are directly addressable, so the Parity bit, or the general purpose flags, for example, are also available to the bit-test instructions.

RELATIVE OFFSET

The destination address for these jumps is specified to the assembler by a label or by an actual address in Program Memory. However, the destination address assembles to a **relative** offset byte. This is a signed (two's complement) offset byte which is added to the PC in two's complement arithmetic if the jump is executed.

The range of the jump is therefore −128 to +127 Program Memory bytes relative to the first byte following the instruction.

Jump Instructions

Table 8 shows the list of unconditional jumps.

Table 8. Unconditional Jumps in MCS®-51 Devices

Mnemonic	Operation	Execution Time (μs)
JMP addr	Jump to addr	2
JMP @A+DPTR	Jump to A+DPTR	2
CALL addr	Call subroutine at addr	2
RET	Return from subroutine	2
RETI	Return from interrupt	2
NOP	No operation	1

The Table lists a single "JMP addr" instruction, but in fact there are three—SJMP, LJMP and AJMP—which differ in the format of the destination address. JMP is a generic mnemonic which can be used if the programmer does not care which way the jump is encoded.

The SJMP instruction encodes the destination address as a relative offset, as described above. The instruction is 2 bytes long, consisting of the opcode and the relative offset byte. The jump distance is limited to a range of − 128 to + 127 bytes relative to the instruction following the SJMP.

The LJMP instruction encodes the destination address as a 16-bit constant. The instruction is 3 bytes long, consisting of the opcode and two address bytes. The destination address can be anywhere in the 64K Program Memory space.

The AJMP instruction encodes the destination address as an 11-bit constant. The instruction is 2 bytes long, consisting of the opcode, which itself contains 3 of the 11 address bits, followed by another byte containing the low 8 bits of the destination address. When the instruction is executed, these 11 bits are simply substituted for the low 11 bits in the PC. The high 5 bits stay the same. Hence the destination has to be within the same 2K block as the instruction following the AJMP.

In all cases the programmer specifies the destination address to the assembler in the same way: as a label or as a 16-bit constant. The assembler will put the destination address into the correct format for the given instruction. If the format required by the instruction will not support the distance to the specified destination address, a "Destination out of range" message is written into the List file.

The JMP @A+DPTR instruction supports case jumps. The destination address is computed at execution time as the sum of the 16-bit DPTR register and the Accumulator. Typically, DPTR is set up with the address of a jump table, and the Accumulator is given an index to the table. In a 5-way branch, for example, an integer 0 through 4 is loaded into the Accumulator. The code to be executed might be as follows:

```
MOV     DPTR,#JUMP_TABLE
MOV     A,INDEX_NUMBER
RL      A
JMP     @A+DPTR
```

The RL A instruction converts the index number (0 through 4) to an even number on the range 0 through 8, because each entry in the jump table is 2 bytes long:

```
JUMP_TABLE:
        AJMP      CASE_0
        AJMP      CASE_1
        AJMP      CASE_2
        AJMP      CASE_3
        AJMP      CASE_4
```

Table 8 shows a single "CALL addr" instruction, but there are two of them—LCALL and ACALL—which differ in the format in which the subroutine address is given to the CPU. CALL is a generic mnemonic which can be used if the programmer does not care which way the address is encoded.

The LCALL instruction uses the 16-bit address format, and the subroutine can be anywhere in the 64K Program Memory space. The ACALL instruction uses the 11-bit format, and the subroutine must be in the same 2K block as the instruction following the ACALL.

In any case the programmer specifies the subroutine address to the assembler in the same way: as a label or as a 16-bit constant. The assembler will put the address into the correct format for the given instructions.

Subroutines should end with a RET instruction, which returns execution to the instruction following the CALL.

RETI is used to return from an interrupt service routine. The only difference between RET and RETI is that RETI tells the interrupt control system that the interrupt in progress is done. If there is no interrupt in progress at the time RETI is executed, then the RETI is functionally identical to RET.

Table 9 shows the list of conditional jumps available to the MCS-51 user. All of these jumps specify the destination address by the relative offset method, and so are limited to a jump distance of − 128 to + 127 bytes from the instruction following the conditional jump instruction. Important to note, however, the user specifies to the assembler the actual destination address the same way as the other jumps: as a label or a 16-bit constant.

ADC0801/ADC0802/ADC0803/ADC0804/ADC0805
8-Bit µP Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters that use a differential potentiometric ladder — similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus with TRI-STATE output latches directly driving the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Differential analog voltage inputs allow increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Features

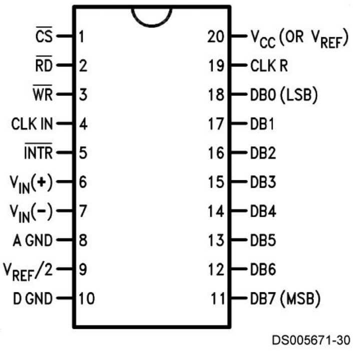
- Compatible with 8080 µP derivatives — no interfacing logic needed - access time - 135 ns
- Easy interface to all microprocessors, or operates “stand alone”
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

Key Specifications

■ Resolution	8 bits
■ Total error	±¼ LSB, ±½ LSB and ±1 LSB
■ Conversion time	100 µs

Connection Diagram

ADC080X
Dual-In-Line and Small Outline (SO) Packages



See Ordering Information

Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity)			
Part Number	**Full-Scale Adjusted**	**V_{REF}/2=2.500 V_{DC} (No Adjustments)**	**V_{REF}/2=No Connection (No Adjustments)**
ADC0801	±¼ LSB		
ADC0802		±½ LSB	
ADC0803	±½ LSB		
ADC0804		±1 LSB	
ADC0805			±1 LSB

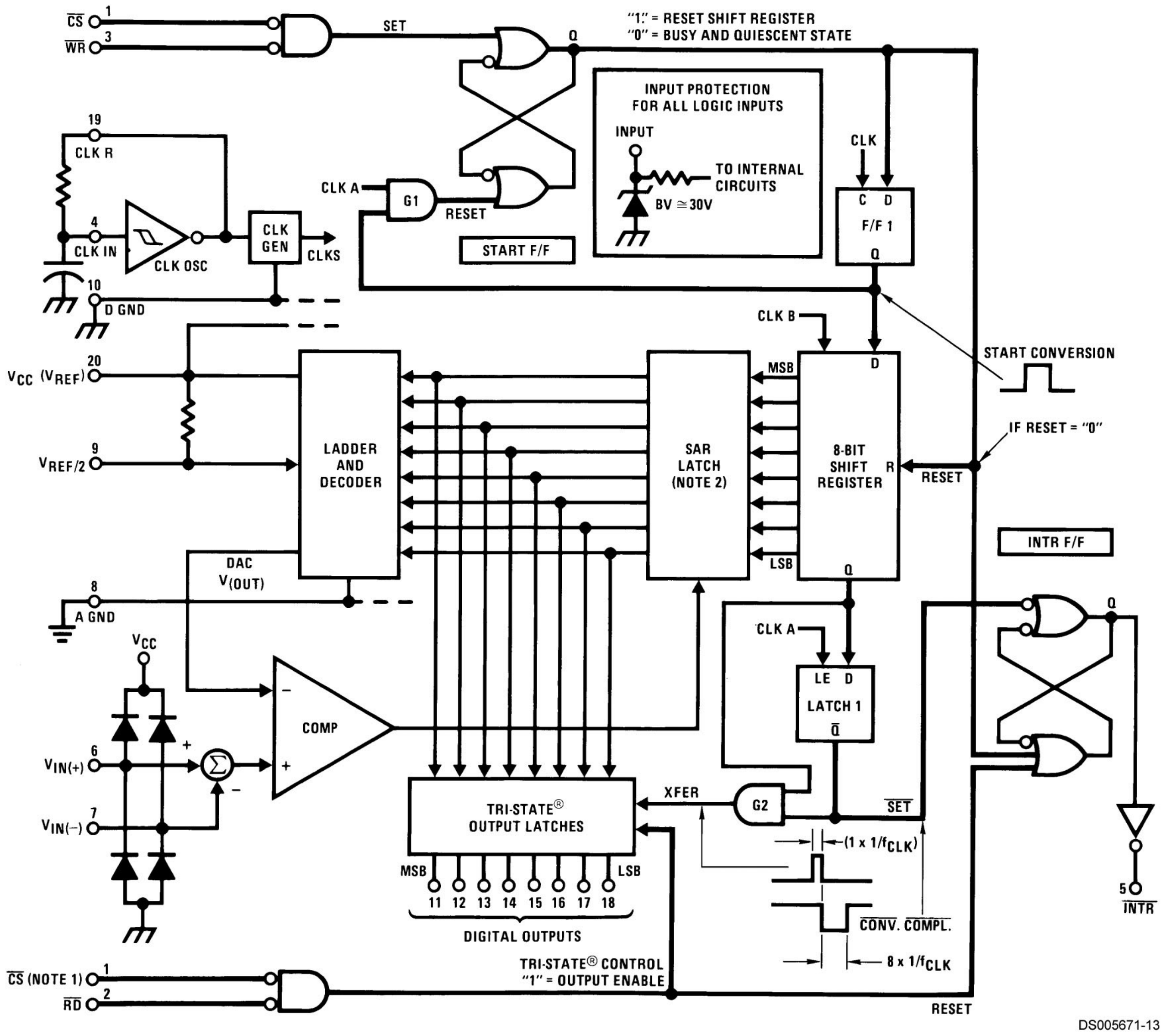
2.0 FUNCTIONAL DESCRIPTION

The ADC0801 series contains a circuit equivalent of the 256R network. Analog switches are sequenced by successive approximation logic to match the analog difference input voltage [$V_{IN}(+) - V_{IN}(-)$] to a corresponding tap on the R network. The most significant bit is tested first and after 8 comparisons (64 clock cycles) a digital 8-bit binary code (1111 1111 = full-scale) is transferred to an output latch and then an interrupt is asserted ($\overline{INTR}$ makes a high-to-low transition). A conversion in process can be interrupted by issuing a second start command. The device may be operated in the free-running mode by connecting $\overline{INTR}$ to the $\overline{WR}$ input with $\overline{CS}$ =0. To ensure start-up under all possible conditions, an external $\overline{WR}$ pulse is required during the first power-up cycle.

On the high-to-low transition of the $\overline{WR}$ input the internal SAR latches and the shift register stages are reset. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. *Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition.*

A functional diagram of the A/D converter is shown in *Figure 4*. All of the package pinouts are shown and the major logic control paths are drawn in heavier weight lines.

The converter is started by having $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting “1” level resets the 8-bit shift register, resets the Interrupt (INTR) F/F and inputs a “1” to the D flop, F/F1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this “1” to the Q output of F/F1. The AND gate, G1, combines this “1” output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a “1”) the start F/F is reset and the 8-bit shift register then can have the “1” clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would momentarily be at a “1” level) and the 8-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{CS}$ and $\overline{WR}$ signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.



Note 13: $\overline{CS}$ shown twice for clarity.

Note 14: SAR = Successive Approximation Register.

FIGURE 4. Block Diagram

After the "1" is clocked through the 8-bit shift register (which completes the SAR search) it appears as the input to the D-type latch, LATCH 1. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the TRI-STATE output latches. When LATCH 1 is subsequently enabled, the Q output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the $\overline{INTR}$ input signal.

Note that this $\overline{SET}$ control of the INTR F/F remains low for 8 of the external clock periods (as the internal clocks run at ⅛ of the frequency of the external clock). If the data output is continuously enabled ($\overline{CS}$ and $\overline{RD}$ both held low), the $\overline{INTR}$ output will still signal the end of conversion (by a high-to-low transition), because the $\overline{SET}$ input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level in this operating mode. This $\overline{INTR}$ output will therefore stay low for the duration of the $\overline{SET}$ signal, which is 8 periods of the external clock frequency (assuming the A/D is not started during this interval).

When operating in the free-running or continuous conversion mode ($\overline{INTR}$ pin tied to $\overline{WR}$ and $\overline{CS}$ wired low—see also section 2.8), the START F/F is SET by the high-to-low transition of the $\overline{INTR}$ signal. This resets the SHIFT REGISTER which causes the input to the D-type latch, LATCH 1, low. As the latch enable input is still present, the $\overline{Q}$ outp go high, which then allows the INTR F/F to be RESET reduces the width of the resulting $\overline{INTR}$ output pulse t a few propagation delays (approximately 300 ns).

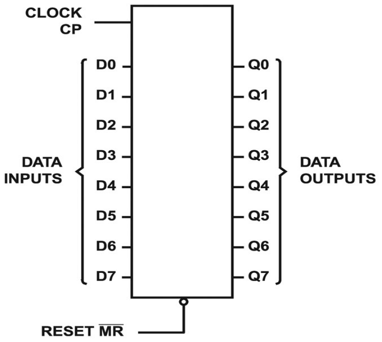
When data is to be read, the combination of both $\overline{CS}$ a being low will cause the INTR F/F to be reset ar TRI-STATE output latches will be enabled to provide th digital outputs.

2.1 Digital Control Inputs

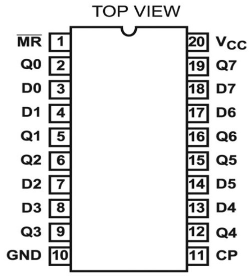
The digital control inputs ($\overline{CS}$, $\overline{RD}$, and $\overline{WR}$) meet sta T^2L logic voltage levels. These signals have been rer when compared to the standard A/D Start and Output E labels. In addition, these inputs are active low to all easy interface to microprocessor control busses non-microprocessor based applications, the $\overline{CS}$ input (can be grounded and the standard A/D Start funct obtained by an active low pulse applied at the $\overline{WR}$ inp 3) and the Output Enable function is caused by an acti pulse at the $\overline{RD}$ input (pin 2).

74HCT273

Functional Diagram



Pınout



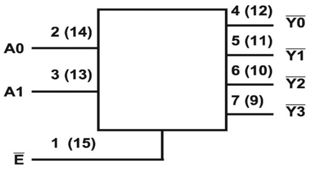
TRUTH TABLE

INPUTS			OUTPUT
RESET ($\overline{MR}$)	CLOCK CP	DATA D_n	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

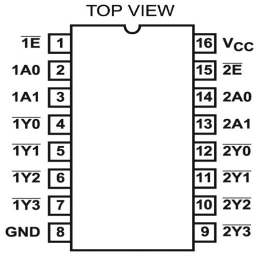
H = High Voltage Level, L = Low Voltage Level, X = Don't Care, ↑ = Transition from Low to High Level, Q_0 = Level Before the Indicated Steady-State Input Conditions Were Established.

74HCT139

Functional Diagram



Pınout



TRUTH TABLE

INPUTS ENABLE SELECT			OUTPUTS			
$\overline{E}$	A1	A0	$\overline{Y3}$	$\overline{Y2}$	$\overline{Y1}$	$\overline{Y0}$
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1
1	X	X	1	1	1	1

X = Don't Care, Logic 1 = High, Logic 0 = Low